BEAM28DI

Quadchannel RX/TX 28GHz Beamforming RFIC

Features

Four channel beamforming transmit receive RFIC featuring over 30dB of amplitude control and phase/ delay control based on digitally programmable delay lines providing 360° of phase control range or at least 24ps of true time delay control.

Built in test equipment for on chip phase and amplitude calibration of the RFIC channels, additionally supporting system calibration.

Applications

Phased Array Transceivers for 5G Communication

Product Validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Description

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1 Product Description

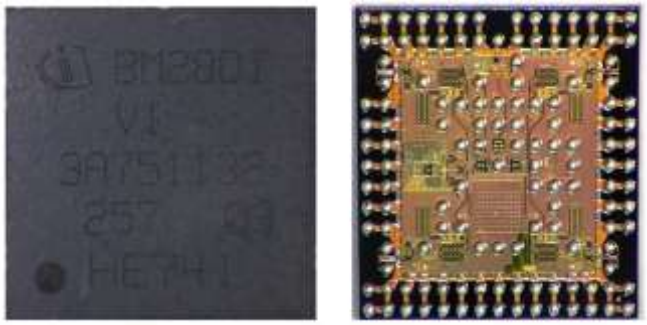

Figure 1 BEAM28DI eWLB Package

The BEAM28DI is a highly integrated quadruple channel transmit receive delay/phase control and amplitude control RFIC for wireless infrastructure applications from 24.25GHz to 30.5 GHz.

- Highly integrated quadruple channel solution
- Bidirectional TDD (Time Division Duplex) RFIC
- Integrated PA, LNA and Rx/Tx switching functionality
- 24.25 to 30.5GHz of digitally configurable RF frequency range supporting up to 800MHz RF instantaneous bandwidth
- 180 degree of programmable phase shift range with an effective resolution of 4 degree in each channel
- +/- 180 degree discrete phase shift realized in the variable amplifiers in each channel
- 24ps of variable relative delay range with an effective resolution of 0.5ps in each channel
- Programable gain amplifiers with more than 30 dB of attenuation range in each amplifier
- Digital control via SCI serial bus
- Fused 48 bit chip identifier supporting calibration and characterization
- Integrated Built-in Test Equipment for on-chip phase and amplitude calibration among the RFIC channels
- Quadchannel total power consumption of max. 2W (85°C) at P1dB CW operation mode
- INFINEON SiGe BiCMOS technology B11HFC (380GHz fmax high performance process)
- eWLB 6.03x6.03mm^2 flip chip partially populated 15x15 bumps package with a ball pitch of 400µm (Fig. 1)

Table 1 Ordering information

Type	Package	Marking	Chip
BEAM28DI	PG-WFWLB-136-2	BM28DIA1	BM28DIA1

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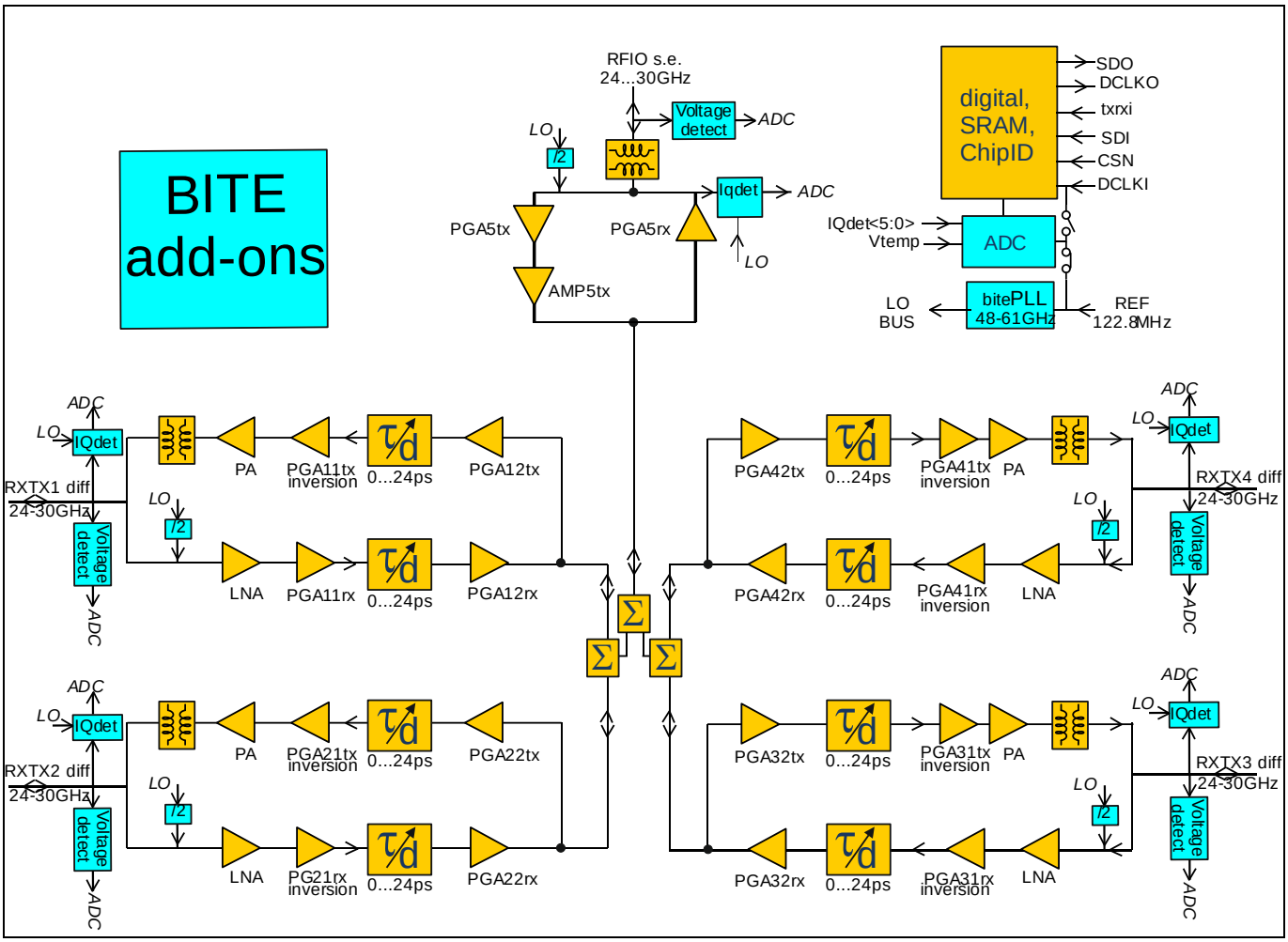

Figure 2 BEAM28DI functional block diagram

2 Package outline and Pin Description

The package has a size of 6.03mm in x-dimension and 6.03mm in y-dimension with a maximum deviation of ±0.1mm in each dimension.
Fig. 3 shows top view, side view and ball positions from the bottom view.
The chip layout and the eWLB ball information is shown in Fig. 4.
The pinning information is shown in Fig. 5. Ball pitch is 400µm.

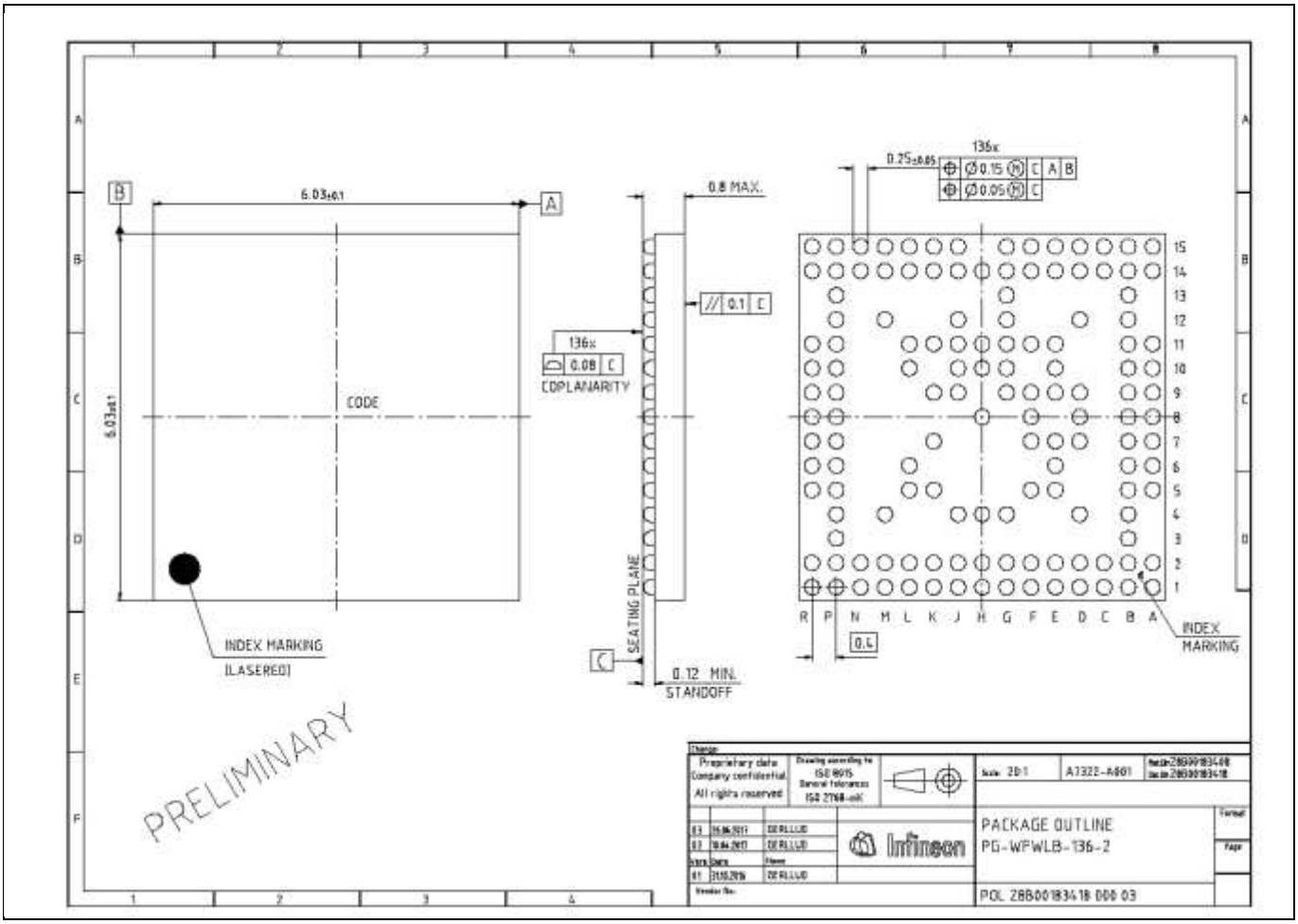

Figure 3 Package outline (Top View, Side View and Bottom View)

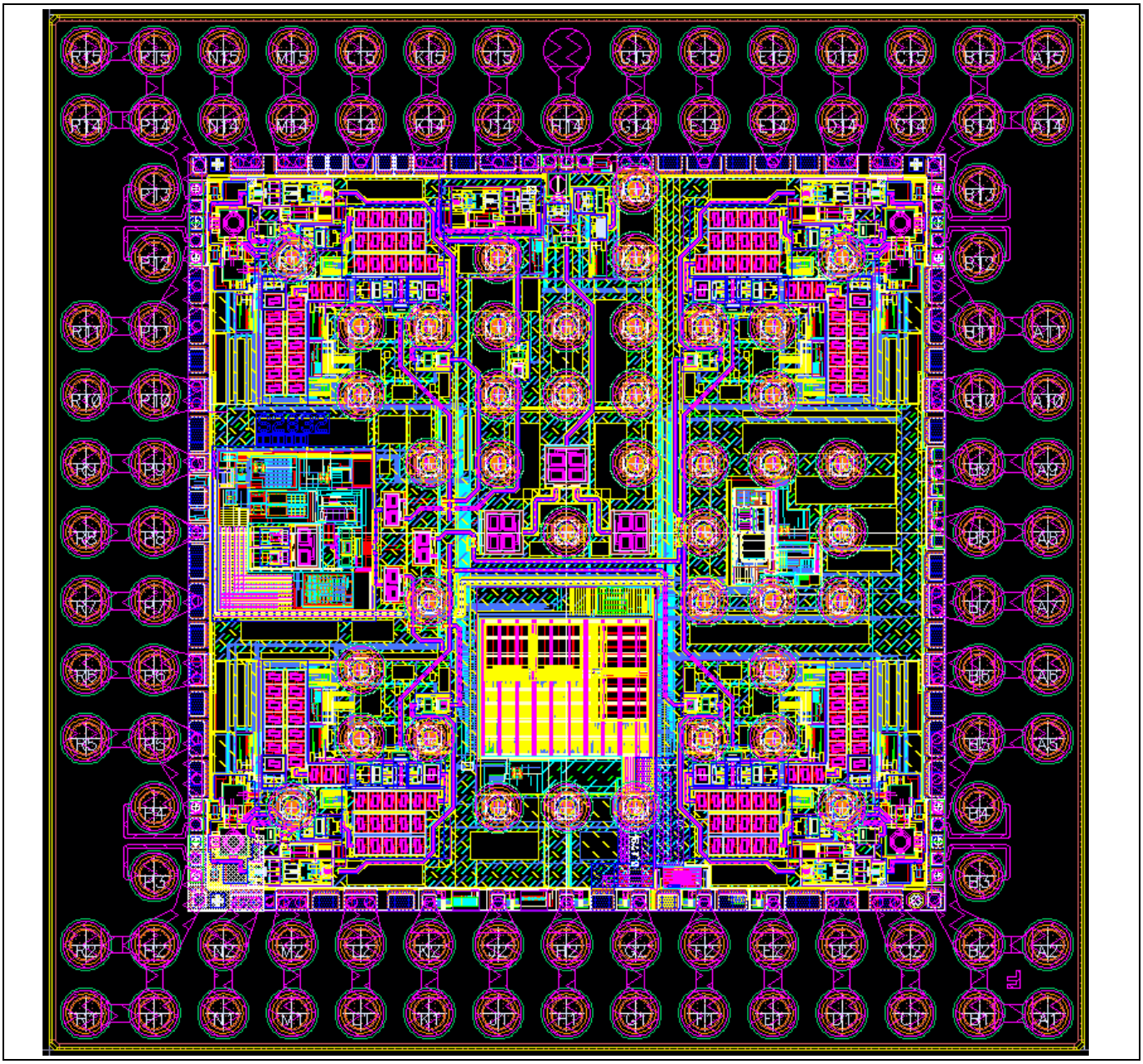

Figure 4 BEAM28DI solder ball side layout view, package size 6.03mm x 6.03mm

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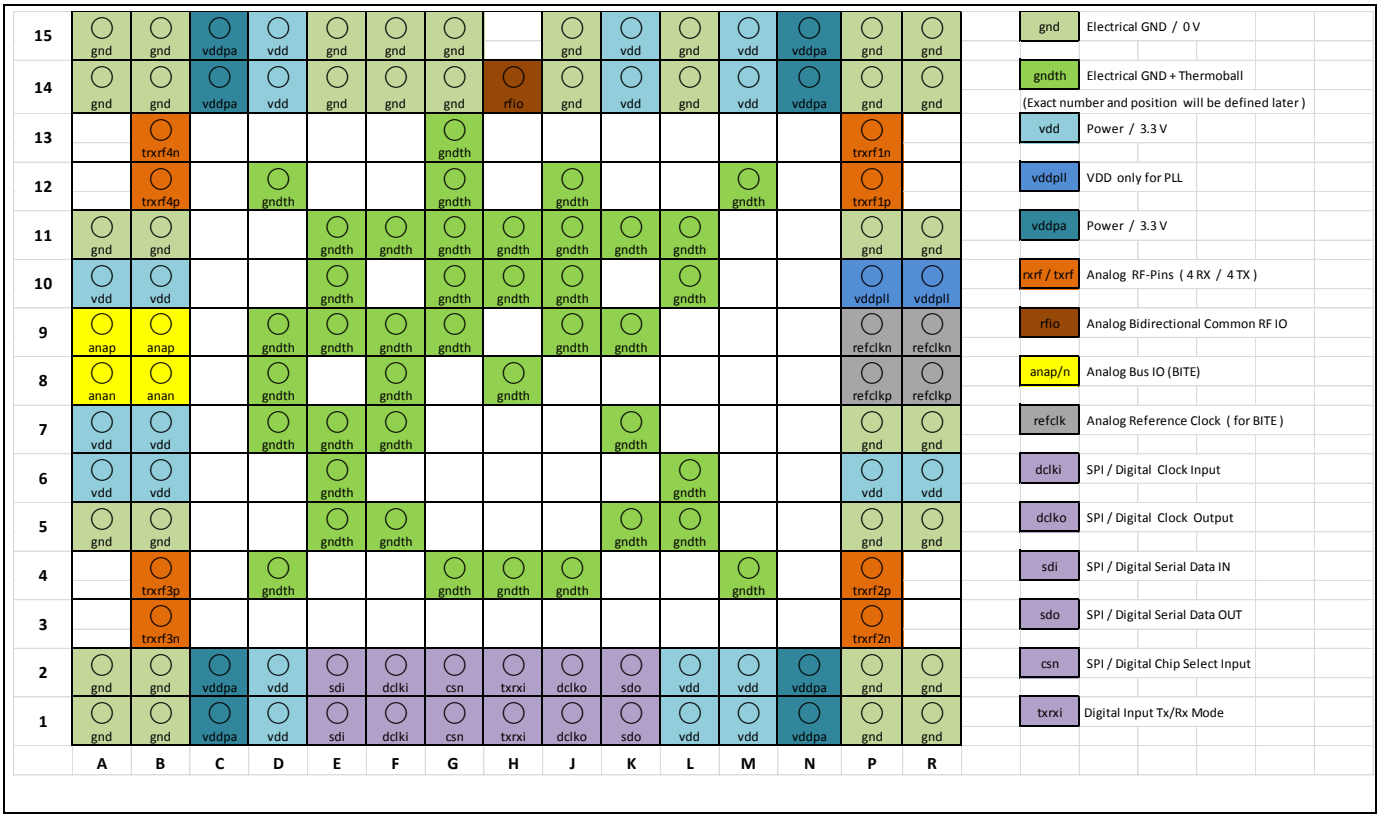

Figure 5 Pin Number Assignment of BEAM28DI package eWLB (Top View)

Table 2 Chip Pads Definition and Function

Pin No.	Symbol	Function	Description
A1, A2, A5, A11, A14, A15, B1, B2, B5, B11, B14, B15, E14, E15, F14, F15, G14, G15, J14, J15, L14, L15, P1, P2, P5, P7, P11, P14, P15, R1, R2, R5, R7, R11, R14, R15	gnd	Power	Electrical ground 0V
D4, D7, D8, D9, D12, E5, E6, E7, E9, E10, E11, F5, F7, F8, F9, F11, G4, G9, G10, G11, G12, G13, H4, H8, H10, H11, J4, J9, J10, J11, J12, K5, K7, K9, K11, L5, L6, L10, L11, M4, M12	gndth	Power	Electrical ground and thermal pads 0V
A6, A7, A10, B6, B7, B10, D1, D2, D14, D15, K14, K15, L1, L2, M1, M2, M14, M15, P6, R6	vdd	Power	DC supply 3.3V
P10, R10	vddpll	Power	PLL DC supply 3.3V low noise
C1, C2, C14, C15, N1, N2, N14, N15	vddpa	Power	DC supply for TX PAs 3.3V
B12	trxrf4p	Bidirectional RF pin of channel 1	analog
B13	trxrf4n	Complementary bidirectional RF pin of channel 1	analog
B4	trxrf3p	Bidirectional RF pin of channel 2	analog
B3	trxrf3n	Complementary bidirectional RF pin of channel 2	analog
P4	trxrf2p	Bidirectional RF pin of channel 3	analog
P3	trxrf2n	Complementary bidirectional RF pin of channel 3	analog
P12	trxrf1p	Bidirectional RF pin of channel 4	analog
P13	trxrf1n	Complementary bidirectional RF pin of channel 4	analog
H14	rfio	Bidirectional common RF input-output pin	analog
A9, B9	anap	Analog input output	Testing pin
A8, B8	anan	Analog input output	Complementary testing pin
P8, R8	refclkp	Analog input	Reference clock for PLL and ADC
P9, R9	refclkn	Analog input	Complementary reference clock for PLL and ADC
F1, F2	dclki	Digital input	SCI clock input
J1, J2	dclko	Digital output	SCI clock output
E1, E2	sdi	Digital input	SCI serial data in

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Pin No.	Symbol	Function	Description
K1, K2	sdo	Digital output	SCI serial data out
G1, G2	csn	Digital input	SCI chip select
H1, H2	txrxi	Digital input	Tx/Rx mode

3 General Product Characteristics

3.1 Maximum Ratings

Stresses above the maximum values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Table 3 Maximum Ratings at T_A=25°C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply Voltage	V_{DD} ,V_{DDPLL}	-0.5	–	3.6	V	–
Storage temperature range	T_{STG}	-55	–	150	°C	–
Junction temperature	T_J	–	–	125	°C	–
Thermal resistance junction – soldering point	$R_{th\text{-}jballs}$	–	2.3		K/W	PCB topside – balls interface (all thermal balls connected)
Thermal resistance junction – topside	$R_{th\text{-}top}$	–	4		K/W	From Si bulk to interface between package and interposer
Maximum DC-voltage on RF-Ports and RF-Ground	V_{RFDC}	0	–	0	V	No DC voltages allowed on RF-Ports
ESD HBM		2			kV	All pins except RF
ESD HBM		0.5			kV	RF pins
ESD CDM		250			V	
TCOB Range		-25		+100	°C	Rogers 3003
TCOB cycles				500		Rogers 3003

3.2 Operational Ratings

The operational ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Table 4 Operational ratings at T_A=25°C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply Voltage	V_{DD}	3.13	3.3	3.47	V	±5%
Supply Voltage	V_{DDPLL}	3.13	3.3	3.47	V	±5%
Clock Duty cycle	DC	45		55	%	
MTTF			1e6		hours	Mean time to failure for T_J range
Junction temperature	T_J	-40		125	°C	MTTF conditions
Ambient temperature PCB	T_{PCB}	-33		95	°C	landing Pad on PCB top-side Functional at -40°C
Lifetime		10			years	T_{PCB} < 85°C continuous operation
PCB RF Isolation		40			dB	RFIO port to any RF-port

4 Electrical Characteristics

4.1 DC electrical characteristics

Table 5 Electrical Characteristics at T_J=25°C and V_{DD} = 3.3V, unless otherwise specified.All voltages refer to GND node.

Parameter	Symbol	Value			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply Voltage	V_{DD} , V_{DDPA}	3.13	3.3	3.47	V	±5%
Supply Voltage	V_{DDPLL}	3.13	3.3	3.47	V	±5%
Supply power receive mode	P_{DDRX}		1.6	2	W	chip RX enabled
Supply power transmit mode	P_{DDTX}		1.6	2	W	chip TX enabled
Supply power BITE PLL	P_{PLL}		270		mW	26mA from vddpll 56mA from vdd pin
Supply power BITE LO bus	P_{LO}		200		mW	from vdd pin
Supply power BITE Detector	P_{phdet}		450		mW	from vdd pin
Supply Power BITE Injector	P_{inj}		350		mW	from vdd pin
Supply power ADC	P_{ADC}			33	mW	from vdd pin
Supply power idle	P_{idle}		10	30	mW	chip disabled

4.2 Common Transmitter and Receiver Characteristics

Table 6 Electrical Characteristics at T_J=25°C and V_{DD} = 3.3V, unless otherwise specified.All voltages refer to GND node. RF performance is characterized including package.

Parameter	Symbol	Value			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Number of channels		4	4	4		Pdc / package limit
RF frequency	f_{RF}	24.25		30.5	GHz	Digitally Configurable
RF instantaneous Bandwidth	BW_{RF}			800	MHz	Newest US target: 1GHz
Channel to Channel isolation			45		dB	Tbc
RF1,2,3,4 ports impedance			100		Ω	active mode, differential
RFIO port impedance			50		Ω	All operation modes, bidirectional, single-ended
Rx to Tx switching time			40	60	ns	Using rxtxmode pin
Inband Gain Flatness		-0.125		0.125	dB	within 100MHz
Inband Gain Flatness		-0.5		0.5	dB	within 800MHz, tbc
Gain control range		30			dB	Total chain RX, Total chain TX
Gain control resolution				0.5	dB	Monotonic
Gain Step Error		-0.25		0.25	dB	

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Parameter	Symbol	Value			Unit	Note / Test Condition
Gain cumulative Error		-0.5		0.5	dB	use BITE to calibrate
Channel to channel gain mismatch		-0.5		0.5	dB	
Gain control settling time				40	ns	within 0.5dB
Channel Gain Phase Error				5	°	At 10dB attenuation
Channel Gain Phase Error				10	°	At 15dB attenuation
Gain variation versus temperature			0.05		dB/°C	
Phase control range total		360			°	
Phase Control No of bits			6+1		bits	0...180° 6bit monotonic + inversion in PGA
Inband phase variation		-1		+1	°	variation from a linear phase within 100MHz
Inband phase variation		-3		+3	°	variation from a linear phase within 800MHz
RMS phase Error			3	5	°	
Channel to channel phase mismatch				1LSB	°	
Relative delay range total		24			ps	21ps delay range + 3ps margin
Relative delay resolution			0.5		ps	
Relative Delay Flatness			2		ps	RMS, within BW_{RF}
Delay variation versus temperature			0.1		ps/°C	absolute, RX and TX
Channel to channel delay mismatch		-0.5		0.5	ps	
Phase/delay control settling time				40	ns	

4.3 Transmitter Characteristics

Table 7 Electrical Characteristics at T_J=25°C and V_{DD} = 3.3V, unless otherwise specified.All voltages refer to GND node. RF performance is characterized including package.

Parameter	Symbol	Value			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RF1,2,3,4 ports matching				-6	dB	Tbc
TX P1dB @ max bias	$P1dB_{TXNOM}$	14	18		dBm	CW, output referred, @maxdelay and maxgain.
TX P1dB control range		10			dB	request for 1W Pdc @ 10dBm
P saturated	P_{sat}		20	21		
TX Gain @ Maximal PGA Gain	$G_{TXMAX25}$	30			dB	Single channel, 25°C
TX Gain @ Maximal PGA Gain	$G_{TXMAX85}$	26			dB	Single channel, 85°C
TX Noise Figure	NF_{TXMAX}		15	18	dB	
TX OIP3	$OIP3_{TXNOM}$	23	25		dBm	Single channel
AM2PM				6	°	Tx, up to P1dB

Parameter	Symbol	Value			Unit	Note / Test Condition
Voltage detector dynamic range	$Vdet_{rng}$		20		dB	Accuracy of +/-2dB
Voltage detector accuracy	$Vdet_{acc}$	-2		+2	dB	Absolute

4.4 Receiver Characteristics

Table 8 Electrical Characteristics at T_j=25°C and V_{DD} = 3.3V, unless otherwise specified.All voltages refer to GND node. RF performance is characterized including package.

Parameter	Symbol	Value			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RF1,2,3,4 ports matching				-10	dB	
RX overload level without damage		0			dBm	CW, single channel
RX Nominal Gain	G_{RX25}	20	22		dB	Single channel operation, all PGA at maximum gain, 25°C
RX Nominal Gain	G_{RX85}	17	19		dB	Single channel operation, all PGA at maximum gain, 85°C
RX IIP3	$IIP3_{RXNOM}$	-20			dBm	input referred, single channel
RX IIP3 3dB Gain Backoff	$IIP3_{RXNOM-3}$		tbd		dBm	input referred, single channel, using channel PGA at $G_{RXNOM-3}$
RX IIP3 3dB Gain Backoff	$IIP3_{RXNOM-3}$		$IIP3_{RXNOM}$		~~dBm~~	input referred, single channel, using PGA5 at $G_{RXNOM-3}$
RX IIP3 10dB Backoff						
RX IIP3 30dB Backoff						
RX OIP3	OIP3rxnom		tbd		dBm	Quadchannel operation
RX IP1dB	$IP1dB_{rx}$	-30				
RX Noise Figure	NF_{RXNOM}		5	7	dB	G_{RXNOM}, single channel including -6dB Wilkinson, $T_j < 85°C$
RX Noise Figure	$NF_{RXNOM-3}$		6	8	dB	$G_{RXNOM-3}$, single channel including -6dB Wilkinson, T_{nom}

4.5 Built in Test Equipment

Table 9 Electrical Characteristics at T_J=25°C and V_{DD} = 3.3V, unless otherwise specified. All voltages refer to GND node. RF performance is characterized including package.

Parameter	Symbol	Value			Unit	Note / Test Condition
		Min.	Typ.	Max.		
PLL reference frequency	f_{REF}	120.8	122.88	124.8	MHz	BITE PLL reference
PLL reference amplitude	V_{REF}	0.5			Vppdiff	BITE
PLL reference input impedance				10	pF	BITE
PLL reference input impedance			2		kΩ	BITE
PLL reference phase noise				-160	dBc/Hz	BITE 20KHz offset frequency
PLL lock time			10	15	µs	BITE
PLL integrated jitter			1		ps	
PLL type		integer-N				BITE
PLL frequency		48.5		61	GHz	
PLL channel raster step			2* f_{REF}		MHz	BITE Integer-N
VCC PLL noise density				10	nV/√Hz	Use e.g. LT3042p
PLL output phase V_{REF} sensitivity			0.5		°/mV	
PLL output phase V_{DD} sensitivity			2		°/mV	
PLL output phase temperature sensitivity			30		°/°C	
Temperature sensor output	T25		A0099x		hex	At 25°C
Temperature sensor slope			4.8		mV/°C	
Temperature sensor accuracy		+5		-5	°C	Absolute temperature

5 BEAM28DI Digital Implementation

5.1 BEAM28DI Controller

5.1.1 Digital/Analog interface

The basic digital IOs are shown in Figure 6. The communication between digital and analog will be in 1.5 Voltage Domain. The 1.5V/3.3V level-shifters are located in the analog macro.

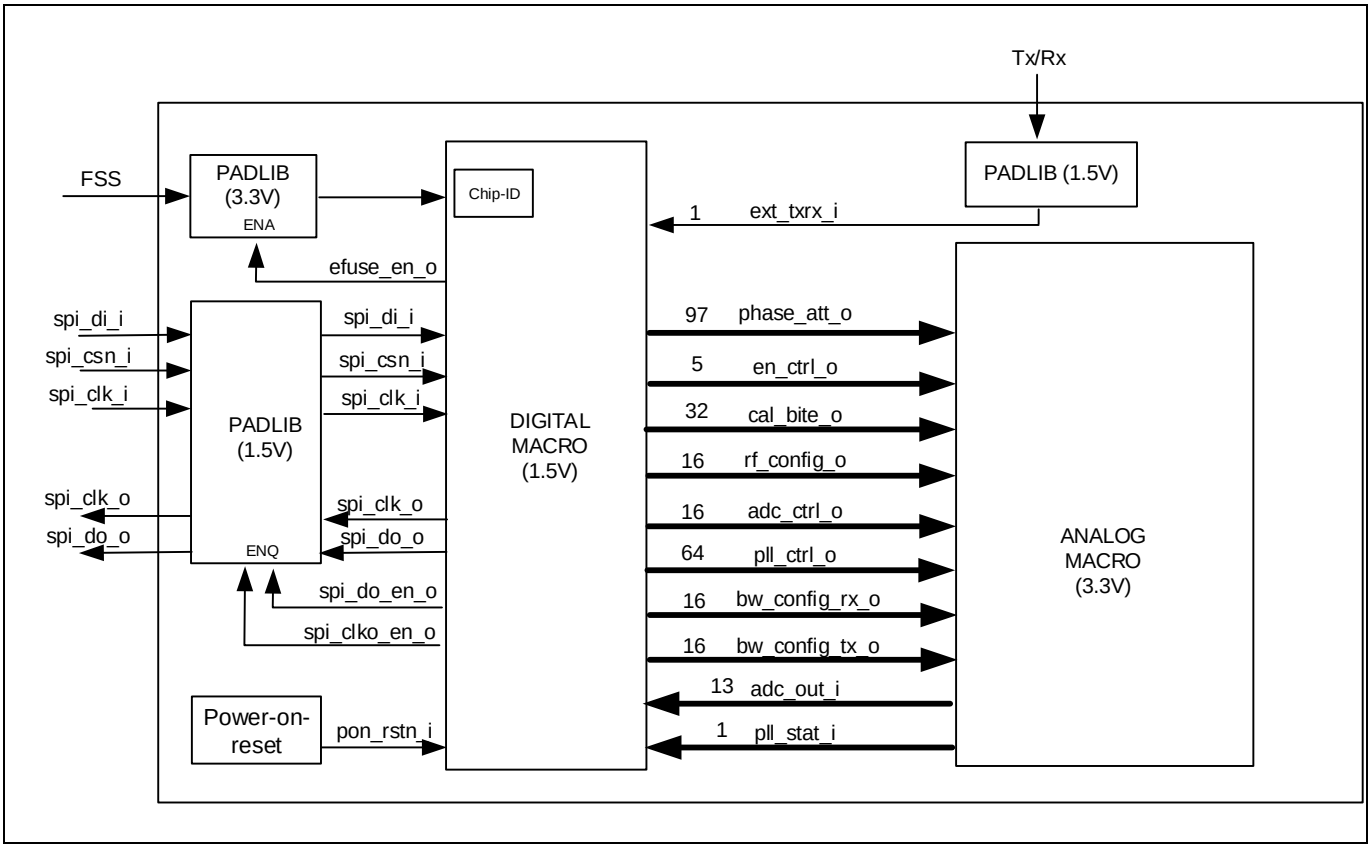


Figure 6 Digital/Analog Interface

SCI_DI: serial data input (master to slave)

SCI_DO: serial data output (slave to master)

SCI_CSN: chip select (low active)

SCI_CLK: clock

5.1.2 BEAM28DI Functional Overview

A more detailed BEAM28DI view which includes the main submodules is shown in Figure 7.

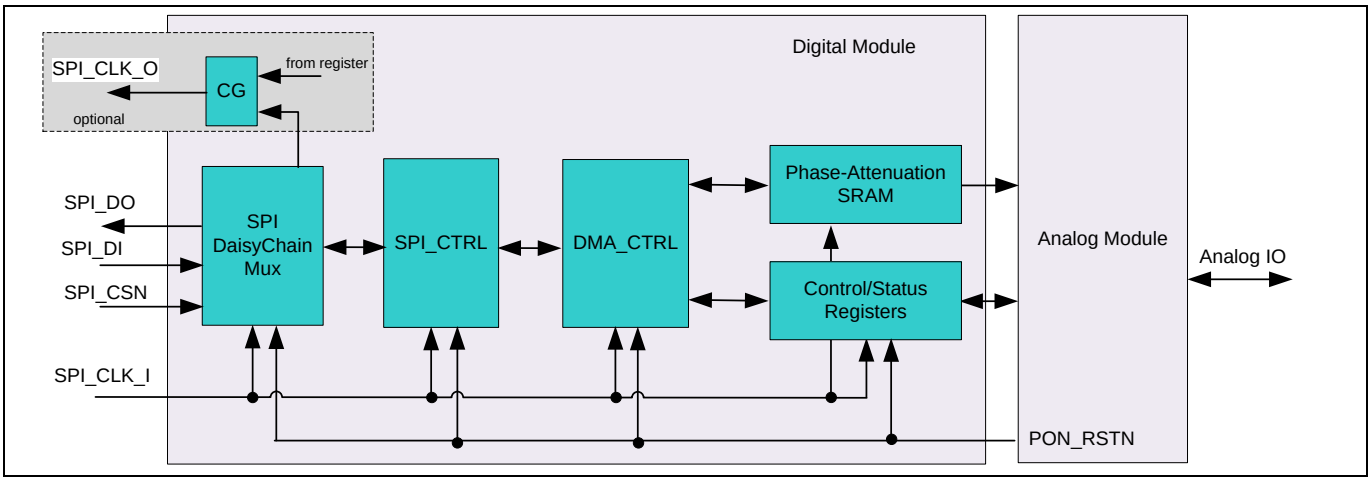


Figure 7 BEAM28DI conceptual diagram

The digital macro contains a non-standard SPI interface (marked as Serial Communication interface or SCI) which transfers data between the BEAM28DI R and the external system control processor. The local control module distributes control and status data to the internal memory which consists of Phase-Attenuation SRAM and a register bank. The Direct Memory Access Control (DMA_CTRL) module controls data distribution from the SRAM memory to the analog macro. The internal scan chain will be inserted for production testing of the digital logic.

5.2 Digital Architecture

5.2.1 Digital Implementation Architecture

The detailed view of the digital controller module is shown in Figure 8.

There are two ways to set a beam configuration: By programming RF_CTRL0-6 registers or by using SRAM. In case RF_CTRL register is used the programming time is tied to a long format of the SCI message and only single configuration (Tx or Rx) is available at the time. Multiple (up to 512) beam configurations could be stored in SRAM. As it's depicted in Figure 8 Phase Attenuation Memory consist of 2 physical memories: SRAM1 and SRAM2. SRAM1 is reserved for 512 Rx configurations and SRAM2 is reserved for 512 Tx configuration. It is important that a pair of Tx/Rx configuration is stored with the same address offset in a corresponding SRAM.

At startup SRAM has to be programmed with SCI long message (note: SRAM access has to be enabled via CONFIG.SPRAM). Once SRAM programming is done, only address pointer (CMD_ADDR) has to be updated with SCI extra-short message during operations to obtain new Tx/Rx settings.

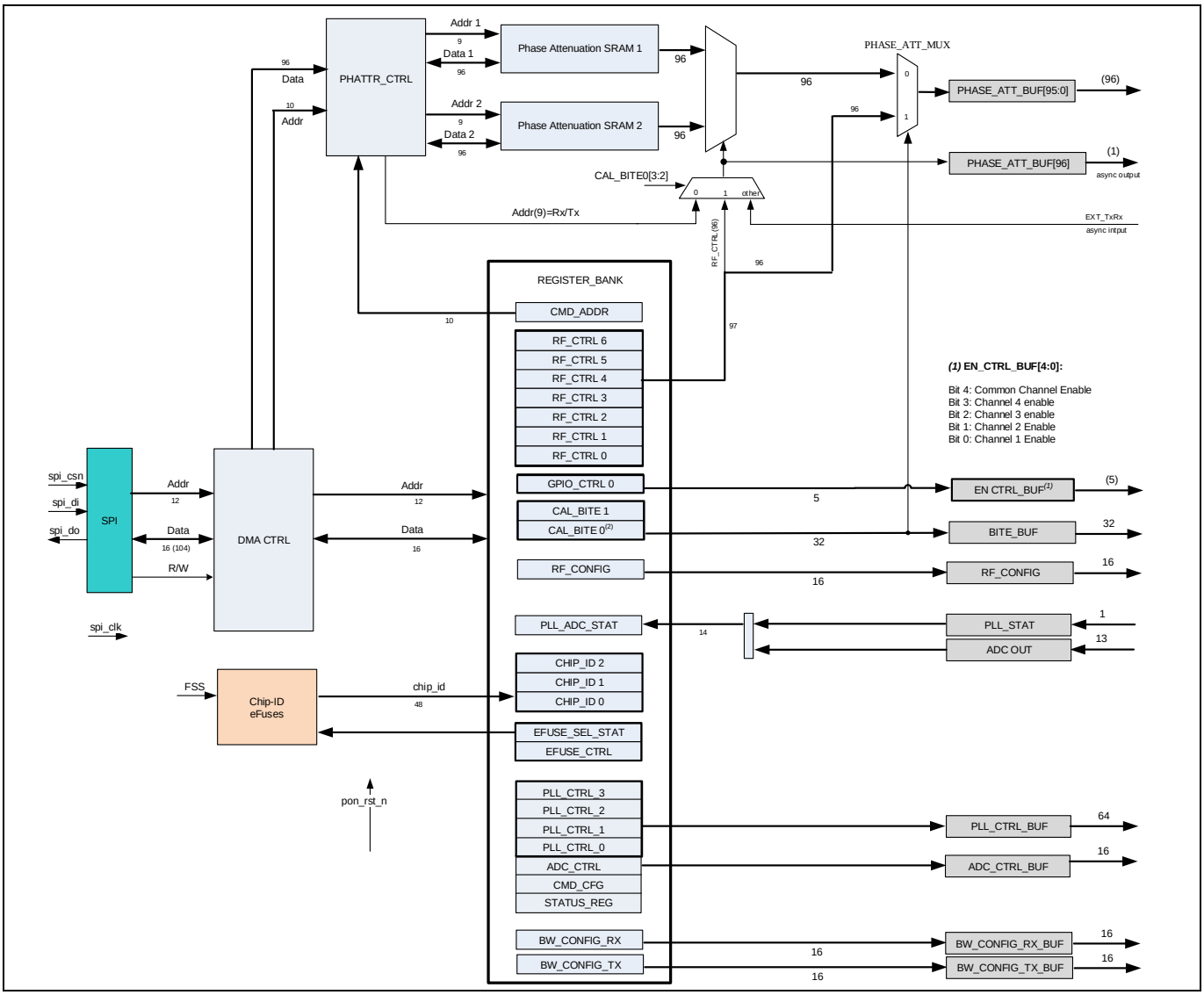


Figure 8 BEAM28DI digital module

5.2.2 SCI Interface

The integrated SCI interface is a full duplex bus with data transfers up to 125 Mbit/s (to be confirmed). This interface defines a protocol and a set of registers that allows 2 devices to communicate directly via data, clock and control lines. This clock frequency allows us to transfer ca. 120 bits within 1 us. The clock line (SCI_CLK) is used for clock synchronization, data line (SCI_DI/SCI_DO) for the data transfers between master and a slave device and the control line (SCI_CSN) is used to control the data transfer and to enable transfer of data to analog macro. This interface allows master and one or more slave devices to communicate to each other. The clock line is a unidirectional connection controlled by the master device. In addition to the single master/slave configuration BEAM28DI supports also the daisy chain operation where the data are shifted in the multiple devices and each device executes the stored command once SCI_CSN gets de-asserted.

SCI interface supports three types of messages (long, short, e-short format) as shown in Figure 9, and 3 kinds of operations (write, read and fast read). Write and read operations are working in both single and daisy-chain modes, while fast read only possible in a single slave mode configuration. In case a fast read programmed in daisy chain configuration a normal read operation will be executed. Timing diagrams of both read operations are shown in Figure 10.

Number of clock cycles when SCI_CSN is 0 that required for data transfer has to be equal to the amount of bits + 1 more clock cycle in the corresponding message format. Active clock (at least 2 clk cycles) after SCI_CSN set to 1 is required when programming/reading SRAM. For programming other registers extra clk cycles are necessary if the SCI cycle error feature is used.

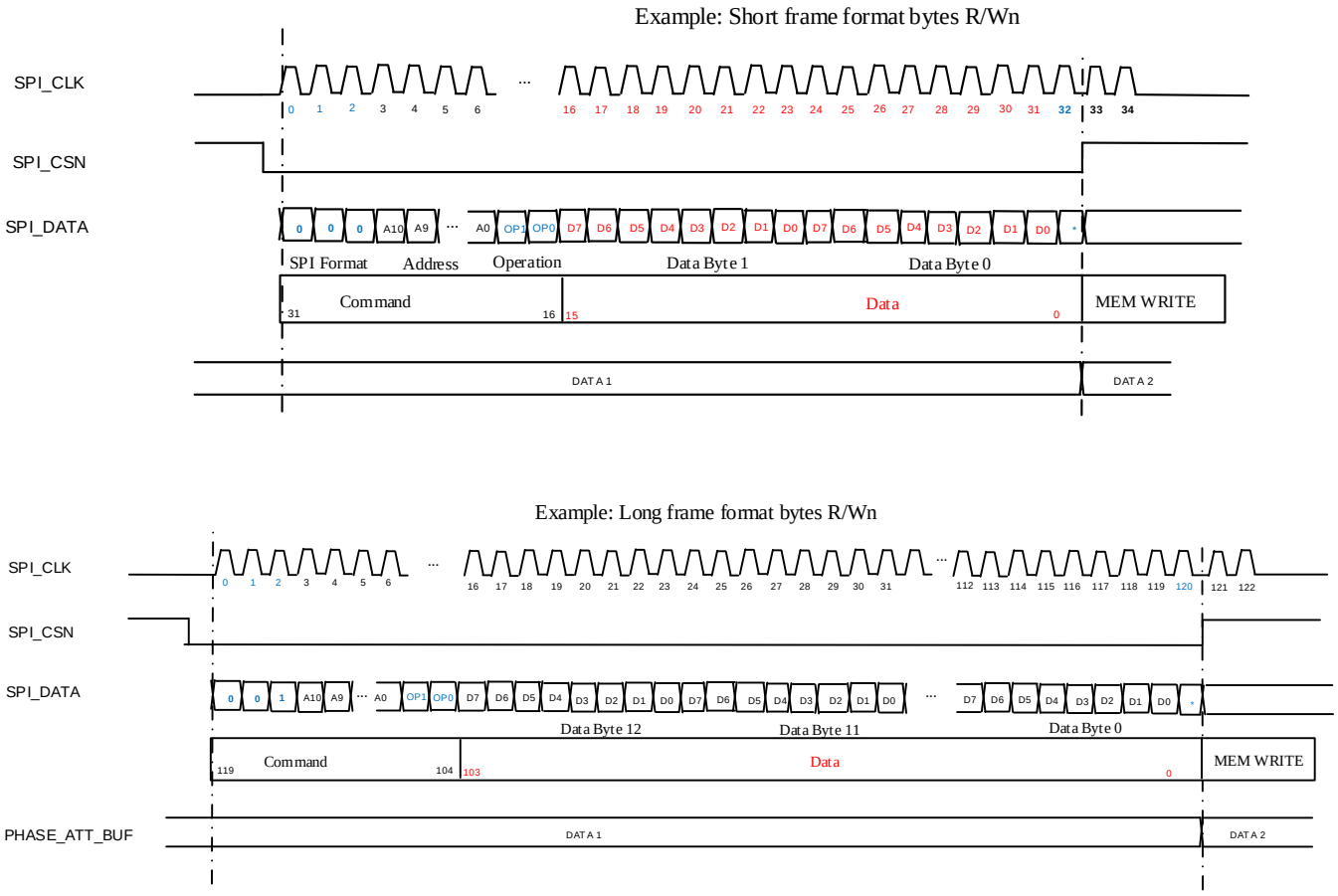


Figure 9 SCI message formats

The SCI interface long format message contains 16 bits command (2 bytes), 104 bits of data (13 bytes) between master and slave. The command byte includes the register/memory address (14 bits) and 2 operation bits. The total number of bytes in the long SCISCI message is 15 (120 bits).

The SCI interface short format message contains 16 bits command (2 bytes), 16 bits of data (2 bytes) between master and slave. The command byte includes the register/memory address (14 bits) and 2 operation bits. The total number of bytes in the short SCISCI message is 4 (32 bits).

The detection of the message format is defined by the address bit 11 (see section 5.2.5.1 BEAM28DI Address Space Summary)

The communication is done bitwise starting with 14 bits of address MSB (A13-A0) followed by 2 operation bits. After sending the command byte the n bytes of payload are sent (MSB first). The complete address range can be accessed through the address extracted from the SCI message.

As it was mentioned before it is possible to have different operations that are configured through operation bits OP1 and OP0 and decoded as following:

OP(1:0) = 00 – write access
OP(1:0) = 01 – read access
OP(1:0) = 10 / 11 – fast read access

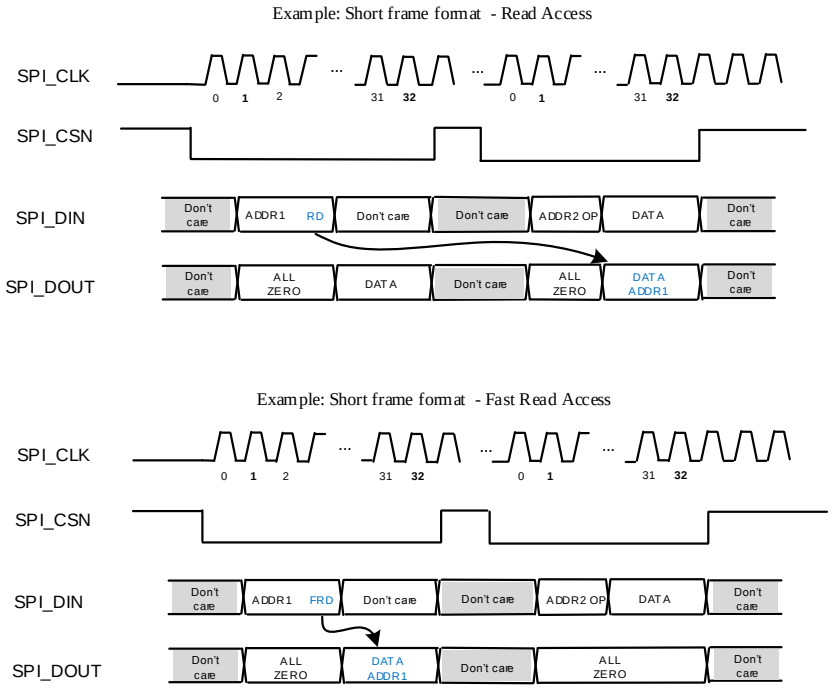


Figure 10 SCI read operation formats

In order to program SRAM a long SCI command has to be used, while a short command is used for programming 16-bit registers. However, it is recommended to program RF Control Register with a long SCI command at once. In this case the SCI message will have a format as shown in Table 10, where CB – command byte, DB – data byte. CB0 and CB1 values are already calculated based on the long message format: “001” (long message format), 0x0A (RF_CTRL0 address) and “00” (write OP). High byte of RF_CTRL6 is reserved and therefore does not require programming. For more details on register bits see *RF_CTRL_0-RF_CTRL_6.*

Table 10 Long SCI command for programming RF_CTRL Register

	CB0	CB1	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
WRITE	0x20	0x28	RF_CTRL6(7:0)	RF_CTRL5		RF_CTRL4		RF_CTRL3		RF_CTRL2		RF_CTRL1		RF_CTRL0	

Depending on an access method, A/D interface parameters update happens with timing delays as depicted in Figure 9. In case a short command is used for updating SRAM address pointer the valid PHASE_ATT_BUF data will be available after 1 clock cycle (address decoding and SRAM read time). In case the content of registers

RF_CTRL0-6 is used as a phase attenuation settings, the PHASE_ATT_BUF data is valid as soon as SCI command has been performed and CSN is set to HIGH.

In case when SRAM is used to store Tx/Rx settings the pointer to next beam configuration is stored in CMD_ADDR register. In order to reduce configuration time of the address pointer an extra-short command has been introduced. The format of this command is shown in Figure 11 and could be used only for programming CMD_ADDR register (OP(1:0) = 00). For read-out of CMD_ADDR the short SCI command is recommended. Once the transfer is done and CSN set to 1, SRAM access will be done to the address programmed in CMD_ADDR register (active clock has to be provided). Corresponding data from the memory will be available at the output after 1 clk cycle.

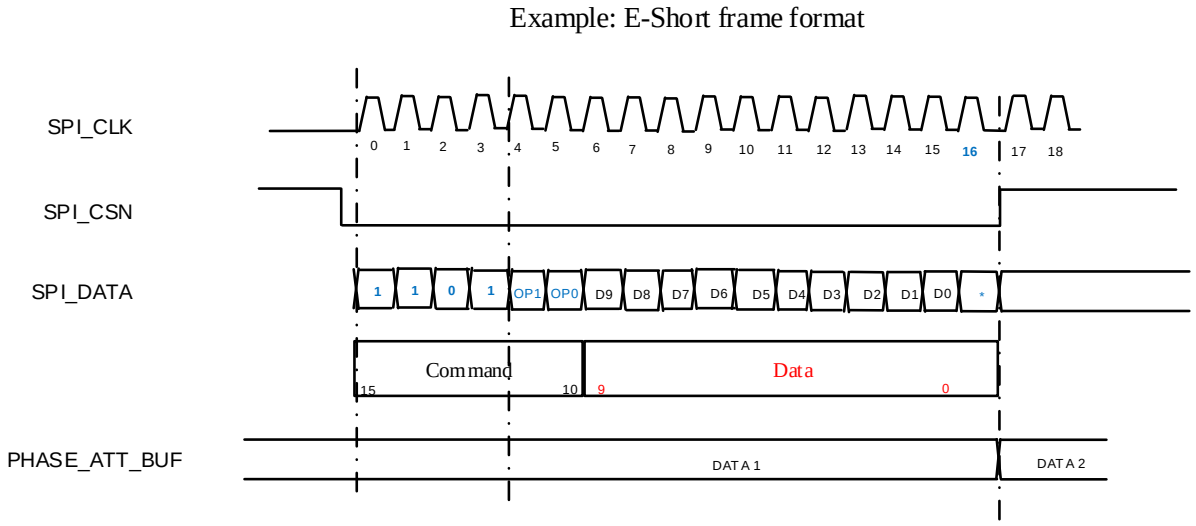


Figure 11 Extra-Short SCI command

5.2.2.1 SCI daisy chain operation

The daisy chain operation is similar to the standard SCI operation except that the BEAM28DI devices are connected in the chain where each device forwards data to the next device in the chain. The master SCI device will need to shift data to/from the complete chain before de-asserting the SCI_CSN signal. The number of bits in the frame depends on a number of devices in the chain and a command format. The number of devices in the chain must be configured in CMD_CFG.DAISY_SIZE. Although there is a possibility to configure up to 8 devices in a chain, it is recommended to use maximum of 4 devices if the clock output SCI_CLKO is used. The command format is SHORT by default and is controlled by DAISY_CMD.TYPE register, which is accessible with any command type and has to be reprogrammed before an access with a different command type is scheduled. The daisy chain system configuration is shown in Figure 12.

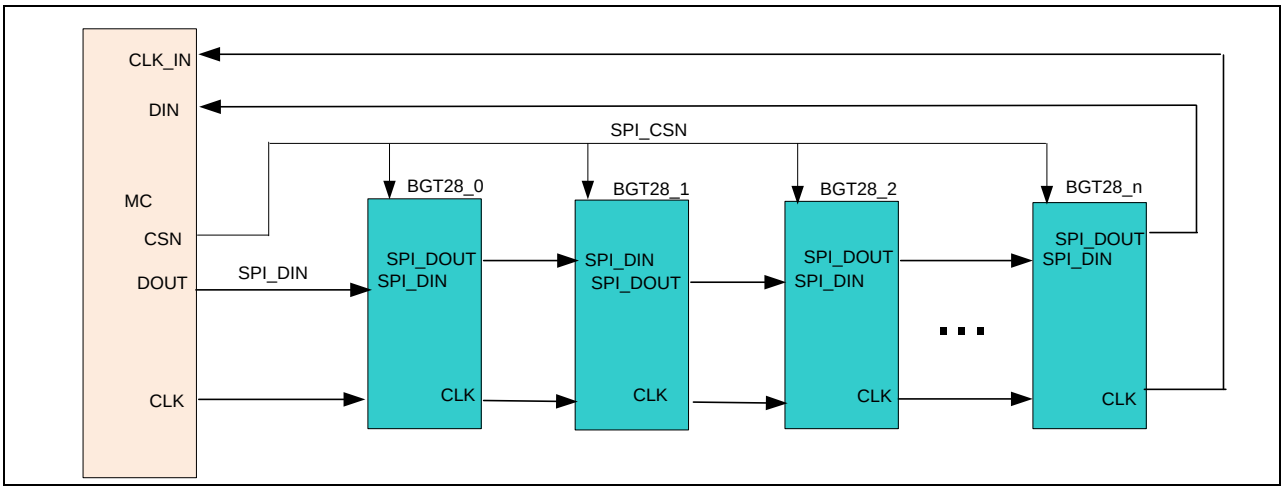


Figure 12 BEAM28DI daisy chain

In order to fulfill the daisy chain operation the external controller shifts data serially depending on the number of devices in the chain and then de-asserts SCI_CSN. The single devices forward data to the next one when SCI_CSN is active and execute the command when internal counter reached an expected value. This value is extracted from a daisy-chain configuration and is equal to an amount of bits to be shifted in the chain (CMDTYPE*DAISY_SIZE). Once the data transfer is finished two more clock cycles should be provided while SCI_CSN is active to execute the command. After this clock should be deactivated and SCI_CSN de-asserted after Tcs(lag). At this time all devices in the chain should have their registers set to the values directed by the external controller.

The external controller has to store data shifted out from the devices in the chain until the last bit gets transferred at which point single device data can be extracted. For the read operation the controller would need to perform second SCI access and continue shift data to the devices in order to get read data from each single device after the shift operation has completed.

It is possible to enable clock propagation through the daisy chain by configuring CMD_CFG.EN_CLKO bit. In case this bit is set clock will be internally buffered and propagated to the output pin, which could be used as input clock signal for the next device in the chain. By default this configuration is enabled.

In order to program all devices in the daisy chain the controller has to perform following steps:

1. Set SCI_CSN to its active level (LOW) and keep SCI_CLK clock inactive
2. Wait for Tco(lead) time before starting SCI CLK
3. Activate SCI_CLK clock
4. Shift in NO_OF_SLAVES*NO_OF_CURRENT_SPI_CMD_CLK_CYCLES + 2 additional bits with the rising edge of the SCI_CLK clock
5. Deactivate SCI_CLK clock
6. Wait for Tco(lag) time
7. Release SCI_CSN to its inactive level (HIGH)

Detailed timing diagram for SCI daisy-chain configuration with 4 devices is shown in Figure 13.

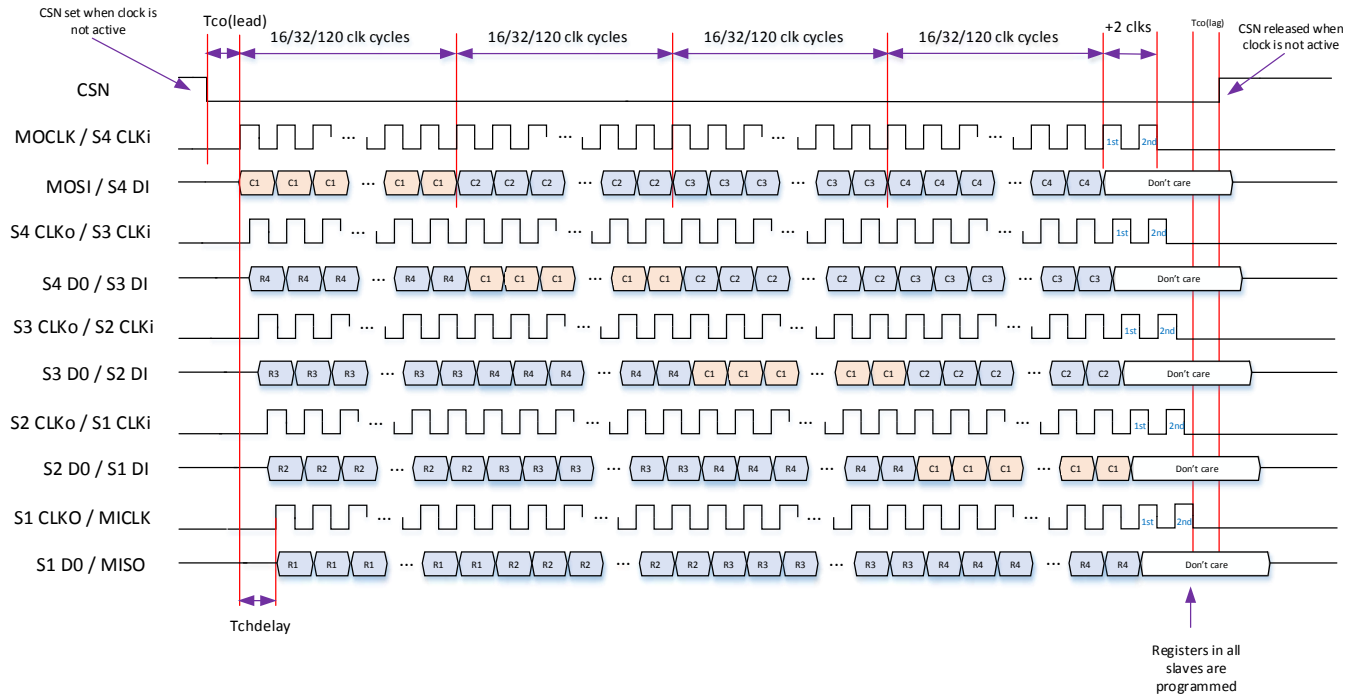


Figure 13 SCI timing diagram for daisy-chain configuration

As it was mentioned before a proper command type has to be selected via DAISY_CMD.TYPE before performing a different command type programming. For instance, the controller programmed ADC_CTRL register in all devices in the chain with SHORT command and in next cycle wants to configure RF_CTRL0-6

with LONG command. In this case before sending LONG command to the chain, controller has to perform a SHORT write operation to DAISY_CMD register to configure properly internal shift registers for LONG command type. Once this operation is done, the controller can proceed with configuring registers and memories, which are accessible by LONG command. In order to switch back to SHORT command DAISY_CMD register has to be reprogrammed back to SHORT command. Same procedure should be applied when switching to/from ESHORT command.

In daisy-chain mode ESHORT command is used for 2 operations:

- Changing SRAM memory pointer for Tx/Rx control, which works as shown in Figure 11 where 4 MSBs should be equal to “1101” followed by 2 OP bits and 10 bits of new SRAM address.
- Reconfiguring DAISY_CMD.TYPE with ESHORT command works slightly different. In this case 4 MSBs should be equal to “1100” followed by 2 OP bits (write only) and 6 bits of ones (0x3F) and 4 LSBs are representing a new command type as shown in below timing diagram after step (4).

(1) In order **to switch from SHORT to LONG** command in daisy chain user has to perform following steps:

1. Set SCI_CSN to its active level (LOW) and keep SCI_CLK clock inactive
2. Wait for Tco(lead) time before starting SCI CLK
3. Activate SCI_CLK clock
4. Shift in **NO_OF_SLAVES*32 bits of data + 2 additional don’t care bits** – This means that we program DAISY_CMD.TYPE register with value ‘0x2’ in each slave
5. Deactivate SCI_CLK clock
6. Wait for Tco(lag) time
7. Release SCI_CSN to its inactive level (HIGH)

(2) In order **to switch from LONG to SHORT** command in daisy chain user has to perform following steps:

1. Set SCI_CSN to its active level (LOW) and keep SCI_CLK clock inactive
2. Wait for Tco(lead) time before starting SCI CLK
3. Activate SCI_CLK clock
4. Shift in **NO_OF_SLAVES*120 bits of data + 2 additional don’t care bits** – This means that we program DAISY_CMD.TYPE register with value ‘0x0’ in each slave
5. Deactivate SCI_CLK clock
6. Wait for Tco(lag) time
7. Release SCI_CSN to its inactive level (HIGH)

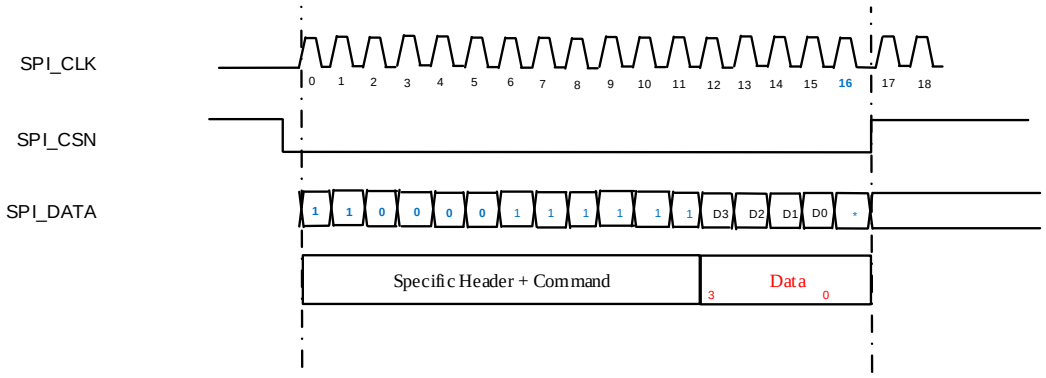
(3) In order **to switch from SHORT to EXTRA_SHORT** command in daisy chain user has to perform following steps:

1. Set SCI_CSN to its active level (LOW) and keep SCI_CLK clock inactive
2. Wait for Tco(lead) time before starting SCI CLK
3. Activate SCI_CLK clock
4. Shift in **NO_OF_SLAVES*32 bits of data + 2 additional don’t care bits** – This means that we program DAISY_CMD.TYPE register with value ‘0x01’ or ‘0x11’ in each slave
5. Deactivate SCI_CLK clock
6. Wait for Tco(lag) time
7. Release SCI_CSN to its inactive level (HIGH)

(4) In order **to switch from EXTRA SHORT to ANY OTHER** command in daisy chain user has to perform following steps:

1. Set SCI_CSN to its active level (LOW) and keep SCI_CLK clock inactive
2. Wait for Tco(lead) time before starting SCI CLK
3. Activate SCI_CLK clock
4. Important: In this case 4 MSB should be equal to "1100" followed by 2 OP bits (write only) and 6 bits of ones (0x3F) and 4 LSB are representing new command type (DAISY_CMD.TYPE)
5. Shift in **NO_OF_SLAVES*16 bits of data + 2 additional don't care bits** – This means that we program DAISY_CMD.TYPE register with value '0x0' or '0x10' in each slave
6. Deactivate SCI_CLK clock
7. Wait for Tco(lag) time
8. Release SCI_CSN to its inactive level (HIGH)

Example: E-Short frame format for programing DAISY_CMD



5.2.2.2 SCI Interface Error Handling

If during any of data exchange sequence an error has been detected the status register lock out bit is set to show failure. In this case analog TX/RX are disabled (EN_CTRL_BUF set to 0x0); any further write commands are blocked until status register has been cleared. This condition is to provide a "hardware safe state" after power on or in case of an error. The power on reset should also cause safe state condition. After the initial start-up-reset, power-on reset or after a lock out state the only way to exit safe state is by clearing the status register including the lock out bit by writing "0xFADE" pattern to STAT_REG register. Following errors will cause the lock out state and lock out bit to be set:

- Phase Attenuation SRAM parity error (STAT_REG. PHATTR_PERR)

STAT_REG also contains some other errors flags that will be set in case of some misbehavior conditions but will not bring the system to the lock out state. Among those are:

- Memory access usage error (STAT_REG.SPRAM_AERR)
- Address Range Error (STAT_REG.ADDR_ERR)
- SCI cycle error (STAT_REG.SCI_CCNT_ERR) – this flag is set when SCI cycle count error is detected and will remain set till any of resets has occurred (single device mode only).

5.2.3 Reset Behavior

BEAM28DI digital macro has three types of resets: reset command via CONFIG register, SCI soft reset via SCI_CSN and an internal reset generated by an internal analog controller at power on or at invalid power supply and provided internally to the digital controller.

Reset command is executed by programming CONFIG.SOFTRES to 1. It is important to keep the clock active for at least 2 cycles after SCI transfer finished and SCI_CSN set to 1. Once the soft reset of the controller has been performed the bit CONFIG.SOFTRES will be automatically cleared.

In case SCI_CSN is active for less or equal 6 SCI_CLK cycles *SCI soft reset* is executed as shown in Figure 14 and SCI slave is reset.

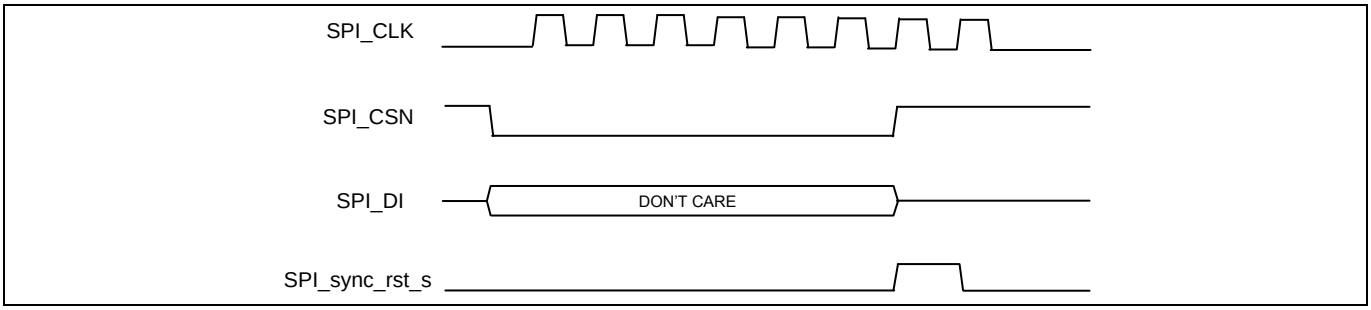


Figure 14 SCI soft reset generation

Power on reset signal is used by digital controller to create the initial reset when powering on and to generate an error condition in case of power loss in the functional mode. If power on reset signal gets asserted during the regular operation the complete digital macro including STAT_REG.PON will be reset to its default value (see *5.2.5.2.1.2*). This way the external controller will be able to detect the STAT_REG.PON being asserted in the regular operation.

The analog power on reset signal pulse is applied asynchronously to reset immediately the digital module and setting analog control signals to the reset values.

After each power on the external controller needs to clear the status register (STAT_REG).

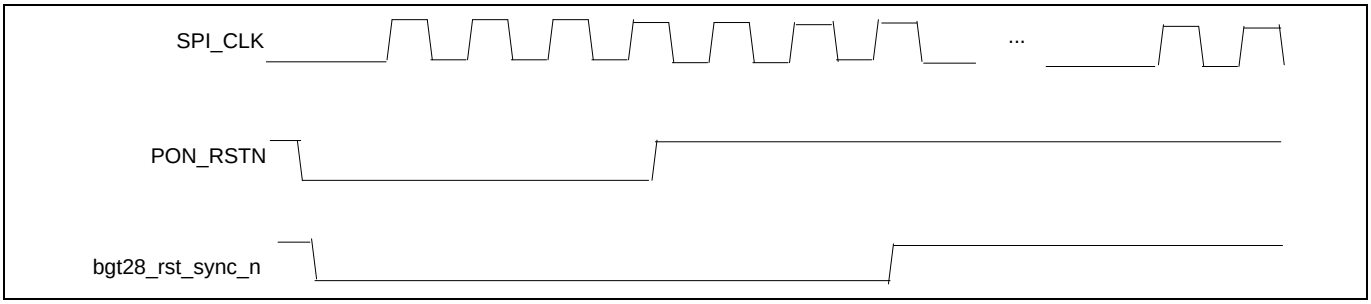


Figure 15 BEAM28DI reset synchronization timing diagram

The asynchronous power on reset is synchronized to the clock by using synchronization mechanism inside design as shown in Figure 16. At the chip level it is important that the first time after powering on the device, while the SPI_CSN is not active, user should run at least 2 SPI CLK cycles on “spi_clk” pin, to get the digital core ready for programming over SPI interface. (Signals “rst_n” and “pon_n” are internal to design)

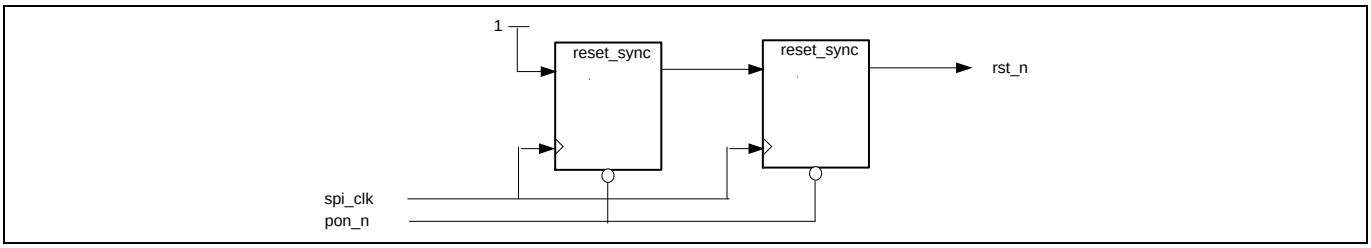


Figure 16 BEAM28DI power on reset synchronization

5.2.4 Design for Test

5.2.4.1 DFT Measures

The following general DFT measures are implemented in BEAM28DI:

- Full scan ATPG
- SPRAM On chip memory MBIST
- Test-access via SCI serial interface
- Analog test via BITE test register

5.2.4.2 Test access control

BEAM28DI uses the SCI interface to access the internal test registers in test mode. The test mode has 2 main access registers: ATPG_CTRL for digital and CAL_BITE for analog tests. The register ATPG_CTRL controls the digital DFT Full Scan ATPG, and the CAL_BITE register controls the settings for analog tests. The analog test results can be read in the register ADC_OUT.

5.2.4.3 Test mode initialization

After the power supply has reached the minimum voltage the power on reset gets released and the test mode can be entered. After release of the power reset the digital controller may be reset using the functional RESETN pin.

5.2.4.4 DFT Architecture

The BEAM28DI has a full-scan capability and achieve 90% stuck-at test coverage (single slave configuration only). The internal memories cannot be directly tested through scan chain and a separate test-mode is used to test them. Since BEAM28DI has a limited pin count only one scan chain is available for testing the complete internal logic. For this reason an internal DFT controller (ipdb_scanctrl) is used to allow integration of the ATPG scan test feature. The basic DFT test architecture is shown in Figure 17. It consists of the ipdb_scanctrl, TCU (Test Control Unit) and MBIST.

The MBIST is controlled by test registers in the TCU. The register bit MBIST_CTRL.MBSTART starts MBIST and the TCU shall read the MBIST from register bit MBIST_CTRL.MBIST_PHATTR_FAIL and MBIST_CTRL.MBDONE.

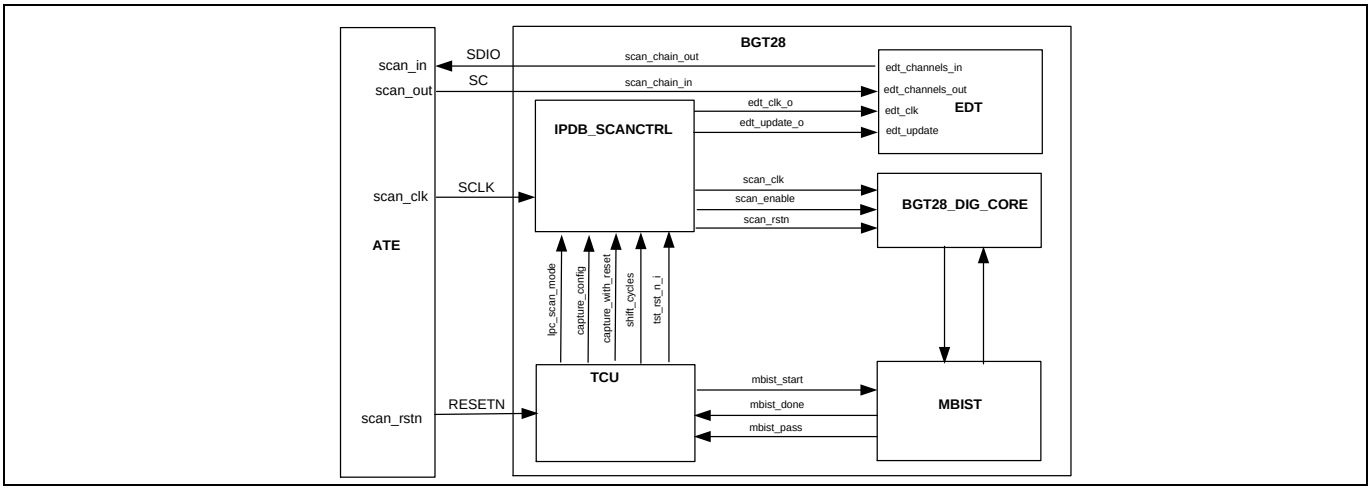


Figure 17 BEAM28DI DFT functional architecture

5.2.5 BEAM28DI Memory Address Map

5.2.5.1 BEAM28DI Address Space Summary

Table 11

Addr Offset	Name	Width 16bit Words	RW	Short Description	Reset	Self Clear	Register/ Memory
0x0000	*CONFIG*	1	RWC	Global Configuration	0x0	N	Register
0x 0001	*STAT_REG*	1	RSC	Global status	0x4080	Y	Register
0x 0002	*CMD_CFG*	1	RW	Command configuration	0x0001	N	Register
0x 0003	*CMD_ADDR*	1	RW	SPRAM address configuration register	0x0	N	Register
0x 0004	*ADC_CTRL*	1	RW	ADC Control	0x0	N	Register
0x 0005	*PLL_CTRL_0*	1	RW	PLL Control 0	0x2004	N	Register
0x 0006	*PLL_CTRL_1*	1	RW	PLL Control 1	0x01A2	N	Register
0x 0007	*PLL_CTRL_2*	1	RW	PLL Control 2	0x0	N	Register
0x 0008	*PLL_CTRL_3*	1	RW	PLL Control 3	0x0	N	Register
0x 0009	*PLL_ADC_STAT*	1	RWC	PLL/ADC Output.	0x0	N	Register
0x 000A	*RF_CTRL_0-RF_CTRL_6*	7	RW	RF path Phase and attenuation	0x0	N	Register
0x 0011	*RF_CONFIG_0*	1	RW	RF path configuration 0	0x0	N	Register
0x 0012	*Reserved*	1	-	Reserved	-	-	Register
0x 0013	*CHIP_ID_0-CHIP_ID_2*	3	R	Chip ID	ID	N	Register
0x 0016	*CAL_BITE_0*	1	RW	Calibration + Bite Control 0	0x0004	N	Register
0x 0017	*CAL_BITE_1*	1	RW	Calibration + Bite Control 1	0x0	N	Register
0x0018	*GPIO_CTRL_0*	1	RW	GPIO control bits 0	0x0	N	Register
0x0019-0x0023	*Reserved*	-	-	Reserved	-	-	Register
0x 0024	*MBIST_CTRL*	1	RW	MBIST Control	0x0	N	Register
0x 0025	*ATPG_CTRL*	1	See reg. details	ATPG control	0x0	N	Register
0x 0026	*ATPG_SHIFT*	1	RW	ATPG shift	0x00CF	N	Register
0x 0027	*BW_CONFIG_Rx*	1	RW	RF cneter frequency config rx	0x0	N	Register
0x 0028	*BW_CONFIG_Tx*	1	RW	RF cneter frequency config tx	0x0	N	Register
0x0029	*EFUSE_SEL_STAT*	1	RW	E-Fuse select and status	0x0	N	Register
0x002A	*EFUSE_CTRL*	1	RWC	E-Fuse control	0x0	Y	Register
0x002B	*DAISY_CMD*	1	RW	SCI command type in daisy chain configuration	0x0	N	Register
0x002C-0x03FF	*Reserved*	-	-	Reserved	-	-	Register (Reserved)
0x0400-0x05FF	*PHATTR1*	512	RW	Phase/Attenuation SRAM 1	-	N	Memory
0x0600-	*PHATTR2*	512	RW	Phase/Attenuation	-	N	Memory

Addr Offset	Name	Width 16bit Words	RW	Short Description	Reset	Self Clear	Register/ Memory
0x07FF				SRAM 2			
0x0800-0x7FFF	*Reserved*	-	-	Reserved	-	-	Memory (Reserved)

5.2.5.2 BEAM28DI Address Space Detail

5.2.5.2.1 Register Address Range

5.2.5.2.1.1 CONFIG

Command/Address Register (see Section 5.2.5)

The Command register is used to specify the type of the access. This register is a self-clear register (RSC). It will always read 0x0.

Table 12

Field	Bits	RW	Reset	Description
RES	[15:14]	R	0x0	Reserved
SPRAM	13	RW	0	SPRAM Memory Access. This bit is set by user when SRAM address range is accessed (see also STAT_REG. SPRAM_AERR).
RES	[12:8]	R	0x0	Reserved
SOFTRES	7	RSC	0	Soft Reset 0: no reset; 1: soft reset
RES	[6:0]	R	0x0	Reserved

5.2.5.2.1.2 STAT_REG

Global status Register (see Section 5.2.5)

The Status register contains the error management status fields. This register can be cleared by writing a special pattern "0xFADE" to this address location.

Table 13

Field	Bits	Reset	Description
RES	15	0	Reserved
PON	14	1	Power on reset has been detected
RES	[13:8]	0x0	Reserved
LOCK	7	1	Lock Out bit. Used to report Lock status. This bit is set on initial power up and in case of an error has been detected (*see section 5.2.2.2)*
RES	[6:4]	0x0	Reserved
SCI_CCNT_ERR	3	0	SPI cycle count error. This bit is set in case an amount of clock cycles during SPI communication is not equal to message length.
PHATTR_PERR	2	0	Phase Attenuation SRAM parity error. This bit is set in case Phase Attenuation SRAM controller detects a parity error.

Field	Bits	Reset	Description
SPRAM_AERR	1	0	Address Error while accessing SPRAM. This bit is set in case of access to SRAM (CONFIG.SPRAM=1) but address is out of SRAM address space or address is in range but CONFIG.SPRAM is not set.
ADDR_ERR	0	0	Address range Error. This bit is set in case of an access to a reserved address location.

5.2.5.2.1.3 CMD_CFG

Command configuration Register (see Section 5.2.5). This register is not affected by synchronous resets. Only PON resets it to a default value.

Table 14

Field	Bits	Reset	Description
DAISY_SIZE	[15:13]	0x0	Number of instances in the daisy chain (max. 8) Encoding: 0x0 = 1 instance (no daisy chain configured) 0x1 = 2 instances in the chain 0x2 = 3 instances in the chain … 0x7 = 8 instances in the chain
RES	[12:1]	0x0	Reserved
EN_CLKO	0	1	Enable clock output and clock propagation through the daisy chain

5.2.5.2.1.4 CMD_ADDR

SPRAM address configuration register.

Table 15

Field	Bits	Reset	Description
RES	[15:10]	0x0	Reserved
ADDR	[9:0]	0x0	Next SPRAM address. This bit field defines the PHATT configuration

5.2.5.2.1.5 ADC_CTRL

ADC control Register (see Section 5.2.5)

Controls the ADCs. The bits depend on the BITE register setting

Table 16

Field	Bits	Reset	Description
CFG_ANA	[15:8]	0x0	Analog switch configuration
EN_ADC	7	0	Enable ADC
GAIN	[6:5]	0x0	ADC gain control, 11b: gain=1.0, 10b gain=0.75, 01b:gain=0.5, 00b: invalid

Field	Bits	Reset	Description
SOC	4	0	Start of Conversion
ODD	3	0	Select odd input
SELLDO<1:0>	[2:1]	0	1.5V Ana Regulator voltage control bits
ADCRESN	0	0	ADC reset, 1: normal operation, 0: reset state

5.2.5.2.1.6 PLL_CTRL_0

PLL control Register 0 (see Section 5.2.5)

PLL Control, Controls the PLLs. The bits depend on the BITE register setting

Column-D shows different voltage domains internal to chip.

Table 17

Field	Bits	Reset	Description	D	
EN_DIV	15	0	Enable VCO and Feedback Divider	1	
SEL_VREF	[14:13]	0x1	select reference voltage for chargepump and loopfilter (500mV nominal)	3	
EN_LF	12	0	Enable Loopfilter	3	
SEL_AMUX	[11:10]	0x0	Select Analog DfT Multiplexer (Current/Voltage Monitors)	3	
EN_AMUX	9	0	Enable Analog DfT Multiplexer	3	
SEL_VCO	[8:7]	0x0	Select VCO	3	
LOGAIN	6	0	reserved	3	
EN_BGP	5	0	Enable Bandgap for PLL bias generation	3	
EN_U2I	4	0	Enable U2I for PLL bias current generation	3	
SEL_VAREG	[3:2]	0x1	Select Bias Current for 1.5V Regulator	3	
EN_REGANA1	1	0	Enable 1.5V regulator for local analog supply domain of PLL	3	
EN_REGDIG0	0	0	Enable 1.5V regulator for local digital supply domain of PLL	3	

5.2.5.2.1.7 PLL_CTRL_1

PLL control Register 1 (see Section 5.2.5)

PLL Control, Controls the PLLs. The bits depend on the BITE register setting

Column-D shows different voltage domains internal to chip.

Table 18

Field	Bits	Reset	Description	D	
SEL_DT	15	0	select amount of dead time delay for phase frequency detector in PLL	1	
FDN_2HI	14	0	Force charge pump DOWN output to static HI	1	
FUP_2HI	13	0	Force charge pump UP output to static HI	1	
FDN_2LO	12	0	Force charge pump DOWN output to static LO	1	
FUP_2LO	11	0	Force charge pump UP output to static LO	1	

Field	Bits	Reset	Description	D	
FFIX_BIA	10	0	Disable charge pump current matching control	1	
SEL_ICP	[9:7]	0x3	Select PLL charge pump current (200uA nominal)	1	
LOCKCTRL	[6:4]	0x2	Lock detection timing error control	1	
SEL_CHN	3	0	Feedback divider static modulus control	3	
SEL_RLF	2	0	Select Loop filter Resistor (2.5kOhm <–> 5k Ohm)	3	
SEL_VDREG	[1:0]	0x2	1.5V Regulator output voltage control bits	3	

5.2.5.2.1.8 PLL_CTRL_2

PLL control Register 2 (see Section 5.2.5)

PLL Control, Controls the PLLs. The bits depend on the BITE register setting

Column-D shows different voltage domains internal to chip.

Table 19

Field	Bits	Reset	Description	D	
FLOCK	15	0	Force Lock-Bit to HI	1	
EN_BOOST	14	0	Boost chargepump current for faster startup	1	
SET_DIV	[13:9]	0x0	integer part of the feedback divider	1	
SWALLOW	[8:5]	0x0	amount of swallows	1	
SEL_DMUX	[4:3]	0x0	Select Digital DfT Multiplexer (fref/fdiv monitoring)	1	
RESN_PLL	2	0	Reset all FFs in PLL (Lockdetection, FB-Counter, ...) –> Low Active!	1	
EN_CP	1	0	Enable Chargepump	1	
EN_DMUX	0	0	Enable Digital DfT Multiplexer	1	

5.2.5.2.1.9 PLL_CTRL_3

PLL control Register 3 (see Section 5.2.5)

Column-D shows different voltage domains internal to chip.

Table 20

Field	Bits	Reset	Description	D
DIVMOD<1:0>	[15:14]	0x0	reserved	3
EX_FOLF	13	0	reserved	1
EX_SELEN	12	0	reserved	1
EX_SELVCO	[11:8]	0x0	reserved	1
EN_LINCAL	7	0	reserved	1
CT_RESN	6	0	reserved	1
CT_ENMON	5	0	reserved	1
EN_RFB3	4	0	Enable PLL RF output Bus 3	3
EN_RFB2	3	0	Enable PLL RF output Bus 2	3
EN_RFB1	2	0	Enable PLL RF output Bus 1	3
EN_QMODE	1	0	reserved	1

Field	Bits	Reset	Description	D
EN_NFILT	0	0	Enable analog noise filters	3

5.2.5.2.1.10 PLL_ADC_STAT

ADC result Register (see Section 5.2.5)

Current ADC output register. This register can be cleared by writing a special pattern "0xFADE" to this address location.

Table 21

Field	Bits	Reset	Description
EOC	15	0	End of ADC conversion use for valid of OUT bits
ADC_OUT	[14:3]	0	ADC Output register. This register holds the digital form of the analog signal currently connected to the ADC input. The selection of bits connected to the ADC input is controlled by CAL_BITE[31:0] register.
RES	[2:1]	0x0	Reserved
PLL_LOCK	0	0	Lock status bit. 1=locked

5.2.5.2.1.11 RF_CTRL_0-RF_CTRL_6

RF Control Register (see Section 5.2.5)

This register set is used to set the RF path Phase and attenuation elements (PHASE_ATT_BUF, Figure 8), when bypassing the Phase attenuation memory. The selection CAL_BITE.PHASE_ATT_MUX = 1 should cause PHASE_ATT_MUX in Figure 8 to use RF_CTRL register as a source for PHASE_ATT_BUF output. This register matches Phase/attenuation control word. It should only be used during BITE and chip evaluation, never during operation.

RF_CTRL mapping .

RF_CTRL[111:96] <-> RF_CTRL_6

RF_CTRL[95:80] <-> RF_CTRL_5

RF_CTRL[79:64] <-> RF_CTRL_4

RF_CTRL[63:48] <-> RF_CTRL _3

RF_CTRL[47:32] <-> RF_CTRL _2

RF_CTRL[31:16] <-> RF_CTRL _1

RF_CTRL[15:0] <-> RF_CTRL _0

Table 22

Field	Bits	Reset	Description
RES	[111:97]	0x0	Reserved
TXMODE	96	0	1: TX mode, 0: RX mode
PHAS4	[95:90]	0x00	Channel 4 phase Control
PHAS3	[89:84]	0x00	Channel 3 phase Control
PHAS2	[83:78]	0x00	Channel 2 phase Control
PHAS1	[77:72]	0x00	Channel 1 phase Control

Field	Bits	Reset	Description
PGA5	[71:64]	0x00	Common channel attenuation and phase inversion control (PGA5)
PGA42	[63:56]	0x00	Channel 4 attenuation and phase inversion control 2 (PGA42)
PGA41	[55:48]	0x00	Channel 4 attenuation and phase inversion control 1 (PGA41)
PGA32	[47:40]	0x00	Channel 3 attenuation and phase inversion control 2 (PGA32)
PGA31	[39:32]	0x00	Channel 3 attenuation and phase inversion control 1 (PGA31)
PGA22	[31:24]	0x00	Channel 2 attenuation and phase inversion control 2 (PGA22)
PGA21	[23:16]	0x00	Channel 2 attenuation and phase inversion control 1 (PGA21)
PGA12	[15:8]	0x00	Channel 1 attenuation and phase inversion control 2 (PGA12)
PGA11	[7:0]	0x00	Channel 1 attenuation and phase inversion control 1 (PGA11)

5.2.5.2.1.12 RF_CONFIG_0

RF Config Register 0 (see Section 5.2.5)

RF_CONFIG [15:0] <-> RF_CONFIG _0

Table 23

Field	Bits	Reset	Description
PA_BIAS_PTAT <15>	15	0	0: CTAT (bias complementary to absolute temperature), 1: PTAT (bias proportional to absolute temperature)
PA_BIAS<14:10>	[14:10]	0x0	PA bias setting
RF_CONFIG_0<9>	9	0x00	AMP5tx bias boost current (+30%)
RF_CONFIG_0<8>	8	0x00	reserved
RF_CONFIG_0<7:0>	[7:0]	0x00	PGA Control Degeneration 0:PGAn1tx 1:PGAn1rx 2:PGAn2tx 3:PGAn2rx 4:PGA5tx 5:PGA5rx 6:AMPn1 7:AMP5tx

5.2.5.2.1.13 BW_CONFIG_Rx

Table 24

Field	Bits	Reset	Description
RXPGA5_IBOOST	15	0	Enable current boost of the RX PGA5
TXPGA5_IBOOST	14	0	Enable current boost of the TX PGA5
RXPGAn2_IBOOST	13	0	Enable current boost of the RX PGAn2
TXPGAn2_IBOOST	12	0	Enable current boost of the TX PGAn2
RXPGAn1_IBOOST	11	0	Enable current boost of the RX PGAn1
TXPGAn1_IBOOST	10	0	Enable current boost of the TX PGAn1
CFREQ_PGAn1	[9:8]	0x0	Center frequency config PGAn1, common for channel n=1,2,3,4rx
PAC2,PAC	[7:6]	0x0	PA cascode impedance control
CFREQ_PGAn2	[5:4]	0x0	Center frequency config connecting Wilkinson and PGAn2rx/tx, common for channel n=1,2,3,4, valid for rx and tx
INJ_GAIN	[3:2]	0x0	Setting gain of the BITE injector

Field	Bits	Reset	Description
			Lowest Gain: 00b Highest Gain: 11b
CFREQ_PGA5	[1:0]	0x0	Center frequency config RFIO transformer, common for channel n=1,2,3,4 rx and tx

5.2.5.2.1.14 BW_CONFIG_Tx

Table 25

Field	Bits	Reset	Description
RES	[15:12]	0x0	Reserved
CFREQ_LNA	[11:10]		Center frequency config LNA, common for all RF channels
CFREQ_PGAn1tx	[9:8]	0x0	Center frequency config PGAn1, common for all RF channels Tx
RES	[7:6]	0x0	Reserved
CFREQ_PGAn2tx	[5:4]	0x0	Center frequency config PGAn2, common for channel n=1,2,3,4tx
RES	[3:2]	0x0	Reserved
CFREQ_PGA5	[1:0]	0x0	Center frequency config output PGA5tx / Center frequency config input PGA5rx, common for channel n=1,2,3,4

5.2.5.2.1.15 CHIP_ID_0-CHIP_ID_2

Chip ID (see Section 5.2.5)

This address location holds the unique chip ID number which is burned in during production (e-fuses). Chip ID cannot be modified at all.

Chip ID mapping:

CHIP_ID[47:32] <-> CHIP_ID_2

CHIP_ID[31:16] <-> CHIP_ID _1

CHIP_ID[15:0] <-> CHIP_ID _0

Table 26

Field	Bits	Reset	Description
CID	[47:0]	Fused CID Value	Unique Chip identifier

5.2.5.2.1.16 CAL_BITE_0

Calibration/Bite register 0 (see Section 5.2.5)

Calibration + Bite registers. Control of BITE/CAL operation / Mux selection (see Figure 8)

CAL_BITE[15:0] <-> CAL_BITE_0

Table 27

Field	Bits	Reset	Description
PHD_SWP	15	0	Phase detector IQ swap
PHD_BW	14	0	Phase detector Integration Bandwidth config 1=ca. 400KHz, 0=ca. 2MHz
GPIO_CON	[13:10]	0x0	reserved
EN_INJ	[9:4]	0x0	Enable /2 Injection<5:0> EN_INJ<5>: reserved EN_INJ<4:1>: Rfport<4:1>. EN_INJ<0>: RFIO port
EXT_TRS_EN	3	0	External input switching between Tx/Rx is enabled
PHASE_ATT_ MUX	2	1	PHASE_ATT_MUX control (see PHASE_ATT_MUX in Figure 8) 0: Data source from Phase attenuation SRAM, PHATTR [95:0] 1: Data Source from register RF_CTRL[95:0].
VREFL	1	0	0: ADC clock from PLL refclk, 1: ADC clock from DCLK pin
VREFH	0	0	Connect internal anabus to ANABUS balls

5.2.5.2.1.17 CAL_BITE_1

Calibration/Bite register 1 (see Section 5.2.5)

Calibration + Bite registers. Control of BITE/CAL operation / Mux selection (see Figure 8)

CAL_BITE[31:16] <-> CAL_BITE_1

Table 28

Field	Bits	Reset	Description
TSENS	15	0	Enable Temperature sensor to Anabus
PD	[14:12]	0x0	Enable and select power detector<4:0> to Anabus
EN_PHD0	11	0	Enable phase detectorPHD0 (5 phase detectors numbered in Figure 2 of Datasheet)
EN_PHD1	10	0	Enable phase detectorPHD1 (5 phase detectors numbered in Figure 2 of Datasheet)
EN_PHD2	9	0	Enable phase detectorPHD2 (5 phase detectors numbered in Figure 2 of Datasheet)
EN_PHD3	8	0	Enable phase detectorPHD3 (5 phase detectors numbered in Figure 2 of Datasheet)
EN_PHD4	7	0	Enable phase detectorPHD4 (5 phase detectors numbered in Figure 2 of Datasheet)
RES	6	0	Reserved
PHD_SELIQ	5	0	Connect phase detector<i> I or Q output to anabus 0:I, 1:Q
PHDSEL	[4:2]	0x0	Connect phase detector<i> output to anabus. 0x0: no connection 0x1: PHD0 … 0x5:PHD4 (phase detectors numbered in Fig. 2 of Datasheet)
CAL_BITE_1<1>	1	0x0	Reserved

Field	Bits	Reset	Description
LDO	[0]	0	Connect VDDDIG to anabus

5.2.5.2.1.18 GPIO_CTRL_0

Direct GPIO Control register 0 (see Section 5.2.5)

This register set is used to set the GPIO_EN_BUF (reserved) and EN_CTRL_BUF (see Figure 8)

GPIO_EN_BUF[9:0] <-> GPIO_CTRL_0[15:6]

EN_CTRL_BUF[4:0] <-> GPIO_CTRL_0[5:1]

Table 29

Field	Bits	Reset	Description
GPIO_EN_9	15	0	Reserved
GPIO_EN_8	14	0	Reserved
GPIO_EN_7	13	0	Reserved
GPIO_EN_6	12	0	Reserved
GPIO_EN_5	11	0	Reserved
GPIO_EN_4	10	0	Reserved
GPIO_EN_3	9	0	Reserved
GPIO_EN_2	8	0	Reserved
GPIO_EN_1	7	0	Reserved
GPIO_EN_0	6	0	Reserved
EN_COM_CH	5	0	Common Channel Enable
EN_CH4	4	0	Channel 4 enable
EN_CH3	3	0	Channel 3 enable
EN_CH2	2	0	Channel 2 enable
EN_CH1	1	0	Channel 1 enable
EN_BGP	0	0	Enable central bandgap buffer

5.2.5.2.1.19 MBIST_CTRL

MBIST Control (see Section 5.2.5)

Memory bist control register.

Table 30

Field	Bits	RW	Reset	Description
PATT	[15:5]	RW	0x0	MBIST entry pattern. MBIST mode will only be entered when MBIST_CTRL.MBSTART is set and this field is equal to 0x5DB
MBRST	4	RSC	0x0	MBIST reset command (High active). This is a self clear bit. It will always read 0
MBIST_PHATTR_FAIL	3	RO	0	MBIST PHATTR pass status 1: MBIST test has failed 0: MBIST test has passed
RES	2	RW	0	Reserved

Field	Bits	RW	Reset	Description
MBDONE	1	RO	0	MBIST completed 1: MBIST test completed 0: MBIST test not completed
MBSTART	0	RSC	0	Start MBIST. MBIST mode will only be entered when this bit is set and the pattern MBIST_CTRL PATT is equal to 0x5DB

5.2.5.2.1.20 ATPG_CTRL

ATPG Control (see Section 5.2.5)

ATPG test control register. This register shall have a gated clock in scan mode.

Table 31

Field	Bits	RW	Reset	Description
PATT	[15:4]	RW	0x0	Scan Entry pattern, the scan mode will only be entered when ATPG_CTRL.SCAN_MODE is set and this field is equal to 0xCAD
RES	[3:2]	RW	0	Reserved
CHAIN	1	RW	0	Chain test mode
SCAN_MODE	0	RW	0	Scan Mode Enable. Scan mode will only be entered when this bit is set and the pattern ATPG_CTRL PATT is equal to 0xCAD

5.2.5.2.1.21 ATPG_SHIFT

ATPG Shift (see Section 5.2.5)

ATPG shift control register.

Table 32

Field	Bits	RW	Reset	Description
CYNR	[15:0]	RW	0x00CE	ATPG number of shift cycles

5.2.5.2.1.22 EFUSE_SEL_STAT

E-fuse select register (see Section 5.2.5)

Table 33

Field	Bits	RW	Reset	Description
EFUSE_PERR	15	RO	0	E-fuse parity error occured
RES	[14:11]	RO	0	reserved
EFUSE_RDY_2	10	RO	0	ChipID2 access finished
EFUSE_RDY_1	9	RO	0	ChipID1 access finished
EFUSE_RDY_0	8	RO	0	ChipID0 access finished
RES	[7:3]	RO	0	reserved

Field	Bits	RW	Reset	Description
EFUSE_SEL_2	2	RW	0	E-fuses for ChipID2 selected
EFUSE_SEL_1	1	RW	0	E-fuses for ChipID1 selected
EFUSE_SEL_0	0	RW	0	E-fuses for ChipID0 selected

5.2.5.2.1.23 EFUSE_CTRL

E-fuse control register (see Section 5.2.5)

This register contains configuration bits for e-Fuse program and read. Programming is done during production test (before packaging). Read is possible at any moment of a device functional mode (see Application Notes for more details).

Table 34

Field	Bits	RW	Reset	Description
RES	[15:5]	R	0	reserved
TESTMODE	4	RW	0	Testmode (production test)
TSTMRGN	3	RW	0	Readout testmargin (TM only)
RDNWR	2	RW	0	Mode: 0 – read access, 1 – write access
STARTPRG	1	RWC	0	Start eFuse programming
ENPRGV	0	RW	0	enable fuse-programming voltage

5.2.5.2.1.24 DAISY_CMD

Command type configuration register in a daisy-chain mode (see Section 5.2.5)

This register contains configuration bits for defining SCI command, which will be used in next access cycle(s). Programming is done one cycle before a new command type is used. This register is accessible with all command types (SHORT/LONG/ESHORT).

Table 35

Field	Bits	RW	Reset	Description
RES	[15:2]	R	0	reserved
TYPE	[1:0]	RW	0	00 – SHORT command type is used in next SCI access 10 – LONG command type is used in next SCI access 01/11 - ESHORT command type is used in next SCI access

5.2.5.2.2 SRAM Address Range

5.2.5.2.2.1 PHATTR1 – PHATTR2

Phase Attenuation control SRAM, [96Kbit] [(96+parity)x512] (see Section 5.2.5)

There are two identical phase attenuation SRAMs. PHATTR1 contains values for Rx configuration, PHATTR2 contains values for Tx configuration. Actual PHASE_ATT value is controlled by CAL_BITE register (see Figure 8)

Table 36

Field	Bits	Description
PAR		Parity bit
PHAS4	[95:90]	Channel 4 phase Control
PHAS3	[89:84]	Channel 3 phase Control
PHAS2	[83:78]	Channel 2 phase Control
PHAS1	[77:72]	Channel 1 phase Control
PGA5	[71:64]	Common channel attenuation and phase inversion control (PGA5)
PGA42	[63:56]	Channel 4 attenuation and phase inversion control 2 (PGA42)
PGA41	[55:48]	Channel 4 attenuation and phase inversion control 1 (PGA41)
PGA32	[47:40]	Channel 3 attenuation and phase inversion control 2 (PGA32)
PGA31	[39:32]	Channel 3 attenuation and phase inversion control 1 (PGA31)
PGA22	[31:24]	Channel 2 attenuation and phase inversion control 2 (PGA22)
PGA21	[23:16]	Channel 2 attenuation and phase inversion control 1 (PGA21)
PGA12	[15:8]	Channel 1 attenuation and phase inversion control 2 (PGA12)
PGA11	[7:0]	Channel 1 attenuation and phase inversion control 1 (PGA11)

5.2.6 Digital Input-Output Specifications

The digital inputs/outputs are designed to be compatible with standard CMOS/TTL levels.

The timing parameters shown in Figure 18 to Figure 20 and specifications in Table 37 have to be considered.

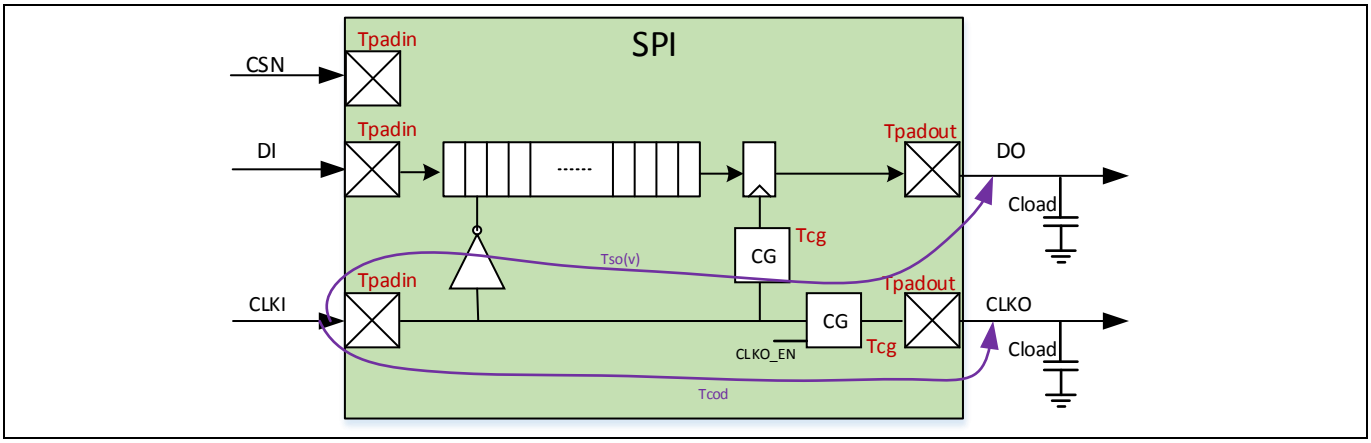


Figure 18 SCI input-output propagation delay

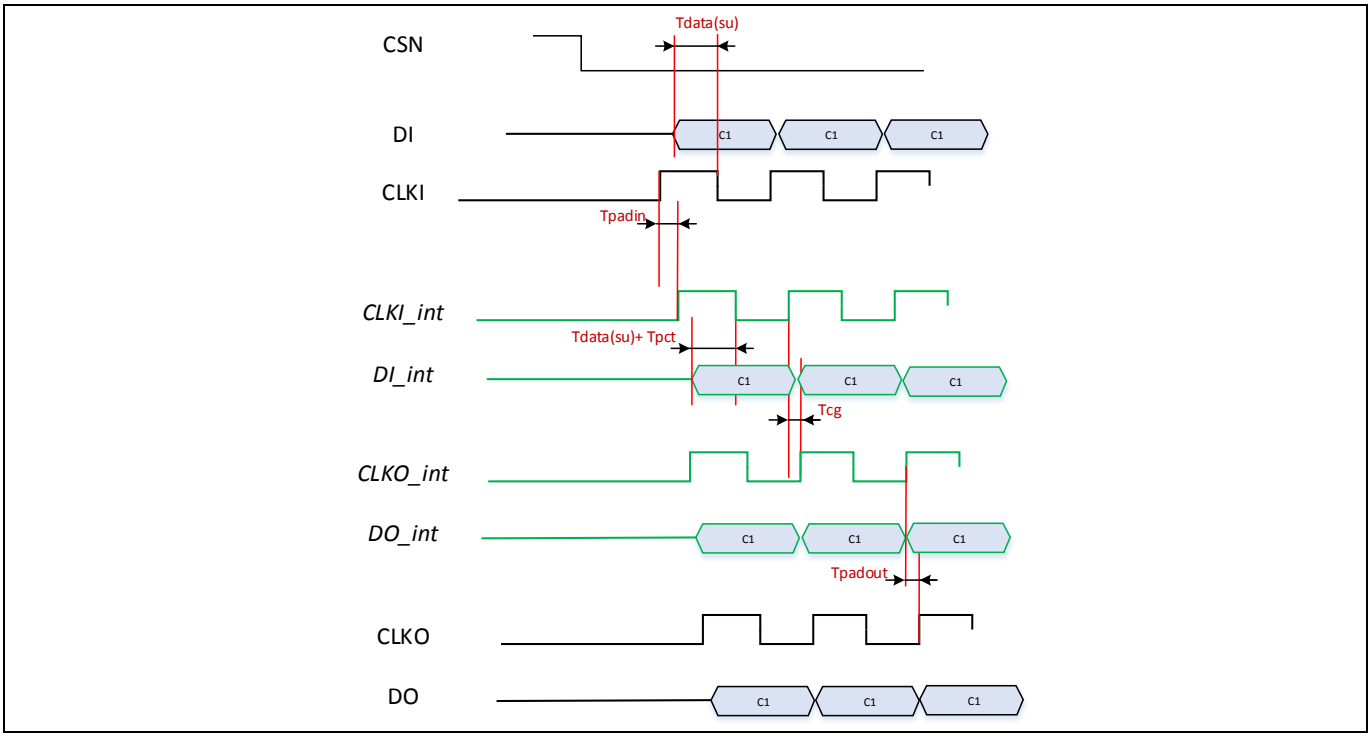


Figure 19 SCI input-output propagation delay timing diagram

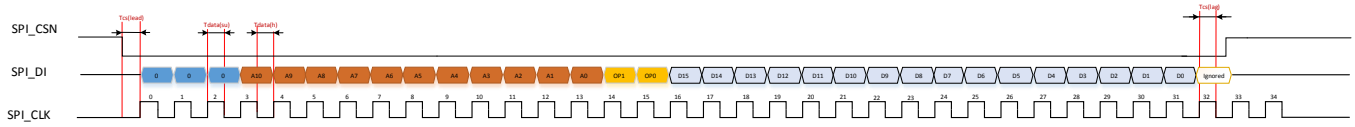


Figure 20 SCI interface timing diagram

In order to program the controller as shown in Figure 20 the user should perform the following steps:

1. Set SPI_CSN to its active level (LOW) and keep SPI_CLK clock inactive

2. Wait minimum for Tcs(lead) time before starting SPI_SCLK
3. Activate SPI_CLK clock
4. Shift in command bits with the rising edge of the SPI_CLK clock
5. Send in one ignore (dummy) bit after the LSB of SPI command data
6. Wait minimum for Tcs(lag) time before deasserting SPI_CSN
7. Deassert SPI_CSN (Set it to HIGH)
8. Keep SPI_CLK active for at least 2 clock cycles
9. Deactivate SPI_CLK clock

Duty-cycle of the input clock has to be at 50% as long as data is transferred. Tcs(lag) is needed for compensating Data and CLK propagation delays through daisy-chain and controlled by the external controller. During Tcs(lag) input clock has to be low. The clock could be held inactive when no data transfer is performed (CSN is HIGH). Single mode configuration requires always additional 2 clock cycles after CSN release. Additional clock cycles after CSN release required only for reset operations (soft resets/ power-on-reset) in daisy-chain mode.

Table 37 Digital SCI IO Timing values at TJ = 25_C, unless otherwise specified

Parameter	Symbol	Values			Unit	Notes
		Min	Typ	Max		
Serial clock frequency	f_{CLK}	none		125 (tbc)	MHz	Minimally 10MHz if used as ADC clock
Serial clock high time	Tclkh			1/2 T_{CLK}	ns	
Serial clock low time	Tclkl			1/2 T_{CLK}	ns	
Chip Select lead time	Tcs(lead)	1/2 T_{CLK}			ns	
Chip Select lag time	Tcs(lag)	11.4			ns	Tchdelay + 1 ns
Input Data Setup Time	Tdata(su)	1.5			ns	
Input Data Hold Time	Tdata(h)	1.5			ns	
Clock Gating Cell delay	Tcg			0.16	ns	
Input PAD delay	Tpadin			1.15	ns	
Output PAD delay	Tpadout			1.3	ns	
CLK to DO valid time	Tso(v)			2.6	ns	load capacitance (C_{LIO})
CLKO to DO skew time	Tskew			1	ns	
Chain propagation time	Tchdelay	10.4				**

**** Propagation time compensation assuming daisy chain configuration with 4 SCI slaves (Tso(v) x 4)**

Table 38 Digital IO Voltage Levels + SCI_O capacitance value at TJ = 25_C, unless otherwise specified

Parameter	Symbol	Values			Unit	Remarks
		Min	Typ	Max		
Input Logic Low	$V_{IN(L)}$	-0.3		0.5	V	
Input Logic High	$V_{IN(H)}$	0.97		1.8	V	
Output Logic Low	$V_{OUT(L)}$	0		0.37	V	I_{OL}=2mA
Output Logic High	$V_{OUT(H)}$	1.12		1.5	V	I_{OH}=-2mA
SCI_O Pad Capacitance	C_{IO}		3 + Cpackage (tbc)		pF	2500fF is die cap only, need to add package parasitics
SCI_O Ext. Load	C_{LIO}			12 (tbc)	pF	

6 Appendix

6.1 PLL Programming

PLL programming flow is shown in 0 All not mentioned PLL related control bits are supposed to be 0. Repeat step 2 & 3 to reprogram a new PLL frequency.

Step 1:	*Bias and PLL Prep*			
	PLL_CTRL Bit Name	Binary Value	PLL_CTRL_#	Bit #
	EN_NFILT	1	3	0
	RESN_PLL	0	2	2
	EN_CP	1	2	1
	LOCKCTRL<2:0>	010	1	6:4
	SEL_RLF	0	1	2
	SEL_ICP<2:0>	100	1	9:7
	SEL_DT	1	1	15
	SEL_VDREG>1:0>	00	1	1:0
	EN_U2I	1	0	4
	EN_BGP	1	0	5
	EN_REGDIG0	1	0	0
	EN_REGANA1	1	0	1
	SEL_VAREG<1:0>	10	0	3:2
	SEL_VREF<1:0>	01	0	14:13
	EN_DIV	1	0	15
	EN_LF	1	0	12
	Program Registers			
	Wait =1ms (Bias to settle)			
Step 2:	*Channel Selection*			
	PLL_CTRL Bit Name	Binary Value	PLL_CTRL_#	Bit #
	RESN_PLL	0	2	2
	SEL_VCO<1:0>	00 … 11	0	8:7
	SEL_CHN	see DIV Table	1	3
	SWALLOW<3:0>		2	8:5
	SET_DIV<4:0>		2	13:9
	Program Registers			
Step 3:	*Enable PLL Locking*			
	PLL_CTRL Bit Name	Binary Value	PLL_CTRL_#	Bit #
	RESN_PLL	1	2	2
	Program Registers			

Figure 21 PLL Programming Flow

The registers settings versus channel frequency for reference frequency of 122.8MHz are shown in Table 39.

Table 39

Channel #	fPLL [MHz]	SEL VCO	SEL CHN	SET DIV	SWALLOW
1	48383.2	00	0	01010	0101
2	48628.8				0110
3	48874.4				0111
4	49120.0				1000
5	49365.6		1	01000	0001
6	49611.2				0010
7	49856.8				0011
8	50102.4				0100
9	50348.0				0101
10	50593.6				0110
11	50839.2				0111
12	51084.8		0	01011	0000
13	51330.4				0001
14	51576.0				0010
15	51821.6				0011
16	52067.2				0100
17	52312.8				0101
18	52558.4				0110
19	52804.0				0111
20	53049.6				1000
21	53295.2				1001
22	53540.8				1010
23	53786.4				1011
24	54032.0		1	01001	0000
25	54277.6				0001
26	54523.2				0010
27	54768.8				0011
28	55014.4	01	0	01100	0000
29	55260.0				0001
30	55505.6				0010
31	55751.2				0011
32	55996.8				0100
33	56242.4				0101
34	56488.0				0110
35	56733.6				0111
36	56979.2				1000
37	57224.8				1001
38	57470.4				1010
39	57716.0				1011
40	57961.6				1100

Channel #	fPLL [MHz]	SEL VCO	SEL CHN	SET DIV	SWALLOW
41	58207.2	01			1101
42	58452.8				1110
43	58698.4				1111
44	58944.0		0	01101	0000
45	59189.6				0001
46	59435.2				0010
47	59680.8				0011
48	59926.4				0100
49	60172.0				0101
50	60417.6				0110
51	60663.2				0111
52	60908.8				1000
53	61154.4				1001

6.2 Abbreviations

All terms and abbreviations relevant for documentation of the Detailed Specification should be recorded here.

Table 40

Term / Abbreviation	Definition / Long form
Component	The term is used in any breakdown of a data processing procedure/system to describe its constituent parts (modules, macros, procedures).

Revision History

Major changes since the last revision

Page or Reference	Description of change
V0.1	Draft Release
V0.2	Minor Changes
V0.3	Minor changes, ESD, package pinning
V0.4	Minor changes
V0.5	Rth top defined, TX voltage detector added, Pinning updated
V0.6	MTTF, package pinning update, PLL lock time, PLL raster, Fig. 2, tbd values defined
V0.7	Pinning update, voltage detector on RFIO port Fig.2, PLL freq, PLL jitter, minor clarifications and typos.
V0.8	Pinning update, Rx NF, Tx Gain
V0.9	Rx Gain, TX gain, NF @ 3dB gain backoff
V0.91	Tx gain increase including additional AMP5tx in block diagram, pinning: digital pins swapped, clock duty cycle, CSO pin removed
V0.92	Chip pads definition
V1.0	Typos, Merge with digital specification, some add. comments in digital specification, P_{idle}

Revision History

Page or Reference	Description of change
V1.1	Reset value of CAL_BITE0 changed, EFUSE_SEL_STAT register updated, update of SCI chapter, balls sdi/dclki/csn reshuffled, clko reset state, amp1tx bit removed, ADC clock multiplexer, *CAL_BITE_0<0> remapped to connect/disconnect anabus to balls,* Digital IO Specification chapter update, typos corrected, coordinates of Bidirectional RF pins corrected in pin description, thermo ball update, added package drawing, parameter of temperature sensor and remark regarding product validation, fixed missing reference links
V1.2	Bit description gpio_ctrl_0<0>, Fig. 20 SCI timing diagram corrections showing first bit being ignored, ADC clock > 10MHz, GPIO_CTRL_REG bit<0> changed to enable central bandgap, RF_CONFIG_0 bit<15> changed to PTAT, BW_CONFIG_TX, BW_CONFIG_RX corrected, Timing diagrams updated for short, long an d extra-short commands, SPI replaced with SCI
V1.3	Change in explanation of Table-36 for PHATTR1 to Rx and PHATTR2 to Tx Correcting RES field bits value of STAT_REG in Table-13 Changed reset value of STAT_REG in Table-11 Changed reset value of PLL_CTRL_0 in Table-11 Removed some unwated column like in Table-18 Timing diagrams of figure 9 updated in section 5.2.2 SCI Interface Timing diagrams of figure 10 updated in section 5.2.2 SCI Interface Timing diagrams of figure 11 updated in section 5.2.2 SCI Interface Description of section 5.2.2.1 SCI daisy chain operation and timing diagram of figure 13 Added timing diagram for programming DAISY_CMD register with ESHORT command Added detailed steps for switching between different SPI commands in daisy chain mode Added more explanation about PON reset synchronization in section 5.2.3 Reset Behaviour Updated MBIST_CTRL field in section 5.2.4.4 DFT Architecture and corresponding change in Table-30 for MBIST_CTRL Updated Timing diagram of SCI interface in figure 20 and corresponding descriptions Picture of eWLB packaged changed
V1.4	Change in minor description of 5.2.2 SCI Interface Update Power On Reset desciption Column-D in Tables-17, 18, 19 and 20 are restored with notes that they represent voltage domains internal to chip. $P1dB_{TXNOM}$ @ maxgain and maydelay conditions Tx and Rx Impedance matching splitted
V1.5	Package pinning ball H14 reworded Section 5.2.1 BEAM28DI Functional Overview SPI/SCI description clarified.
V1.6	ATPG_CTRL Reset value, description of RF frequency coverage clarified as digitally configurable, tbd values for relative delay flatness and channel gain flatness replaced by measured numbers. PLL output phase sensitivity tbd replaced by numerical values , BITE PLL power consumption, Lifetime and PCB isolation additional spec., Registers BW_CONFIG_Tx and BW_CONFIG_Rx bit descriptins corrected.

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